

MS-7509

VER 10
uATX(244mm X 200mm)

CPU:

AMD AM2+ Socket940

System Chipset:

North Bridge --- / MCP78

South Bridge --- NA

OnBoard Chipset:

Clock Gen:NA

AC'97 Codec:ALC888

LAN Chip: REL8211BL/8201CL

SIO:Fintek 882(with smart fan control-3/4 pin co-lay)

Flash ROM:8MB SPI (SIO)

Main Memory:

DDRII* 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

PCI Slot * 2

PWM:

Controller:ISL6566

ACPI:

UPI solution

Other:

FDD *1

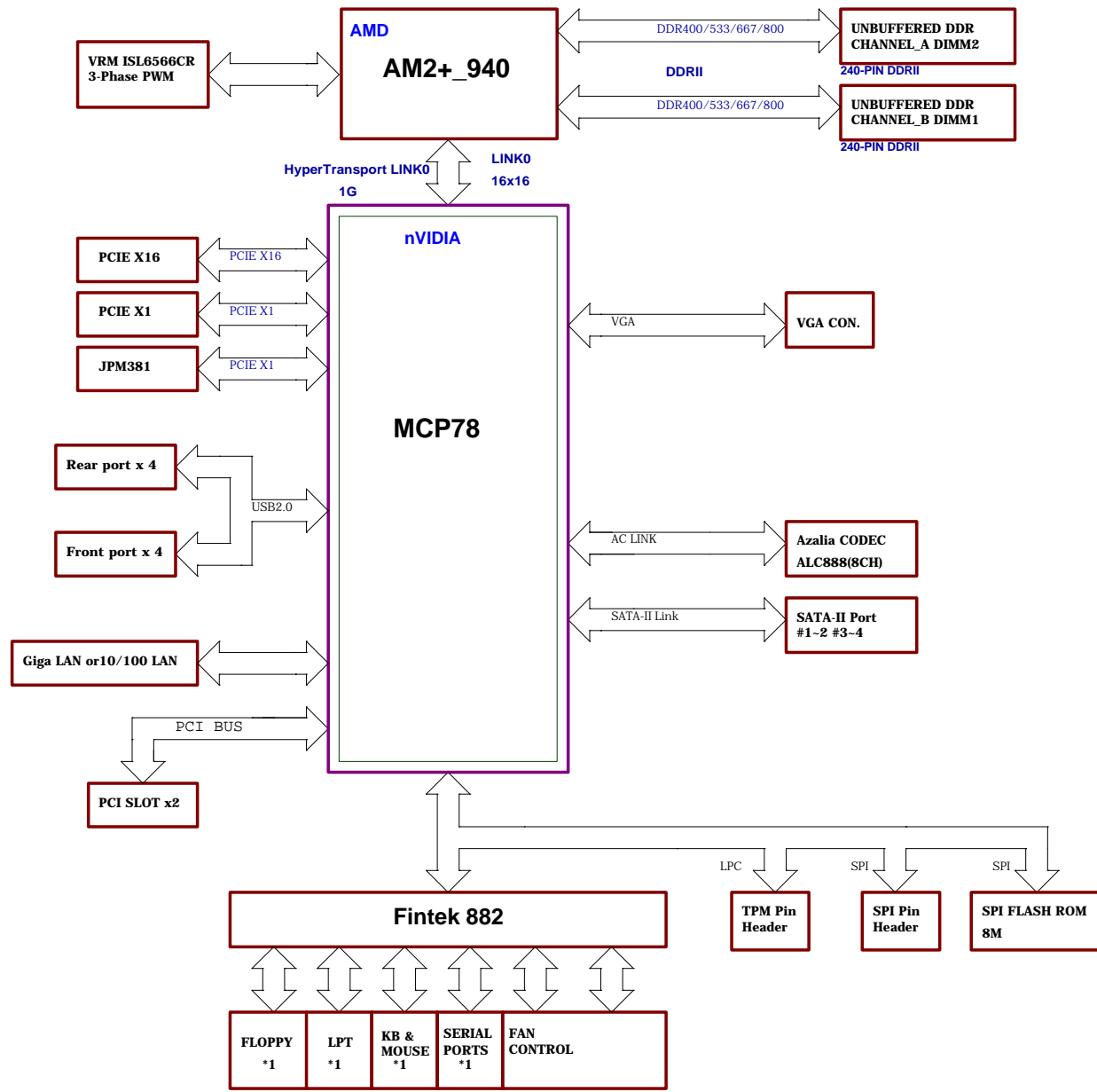
SATA(SATA2-300MB/s) * 4

USB2.0 *8 (Rear*4 Front*4)

COM PORT *1

LPT PORT *1

Title	Page
Cover Sheet	1
Block Diagram	2
Device Map	3
GPIO Table	4
Clock Distribution	5
CPU: AM2+	6,7,8,9
DDR2 DIMM(Dual Channel)	10,11,12
MCP78	13 ~ 19
LAN_ RTL8211BL/8201CL	20
PCIE x 16 , x1 Slots.	21
PCI Slot1 / 2	22
VGA connect	23
FAN	24
USB Conn.	25
Azalia Codec	26
SIO-F71882FG / TPM	27
KB/MS&COM1&LPT&Floppy Conn.	28
ACPI Power Controller-UPI	29
UPI 6103 System Regulators	30
VRM-ISL6566	31
Front Panel	32
For EMI	33
BOM - Option Parts	34
Power Delivery	35
Power Sequence	36
History	37



DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2

USB	Port	DATA +/−	OC#
Rear	LAN_USB1	USB0− USB0+ USB1− USB1+	OC#0
	I1394_USB1	USB2− USB2+ USB3− USB3+	OC#1
Front	JUSB1	USB4− USB4+ USB5− USB5+	OC#2
	JUSB2	USB6− USB6+ USB7− USB7+	OC#3
		USB8− USB8+ USB9− USB9+	OC#4 ~5
		USB10− USB10+ USB11− USB11+	

PCI Config.

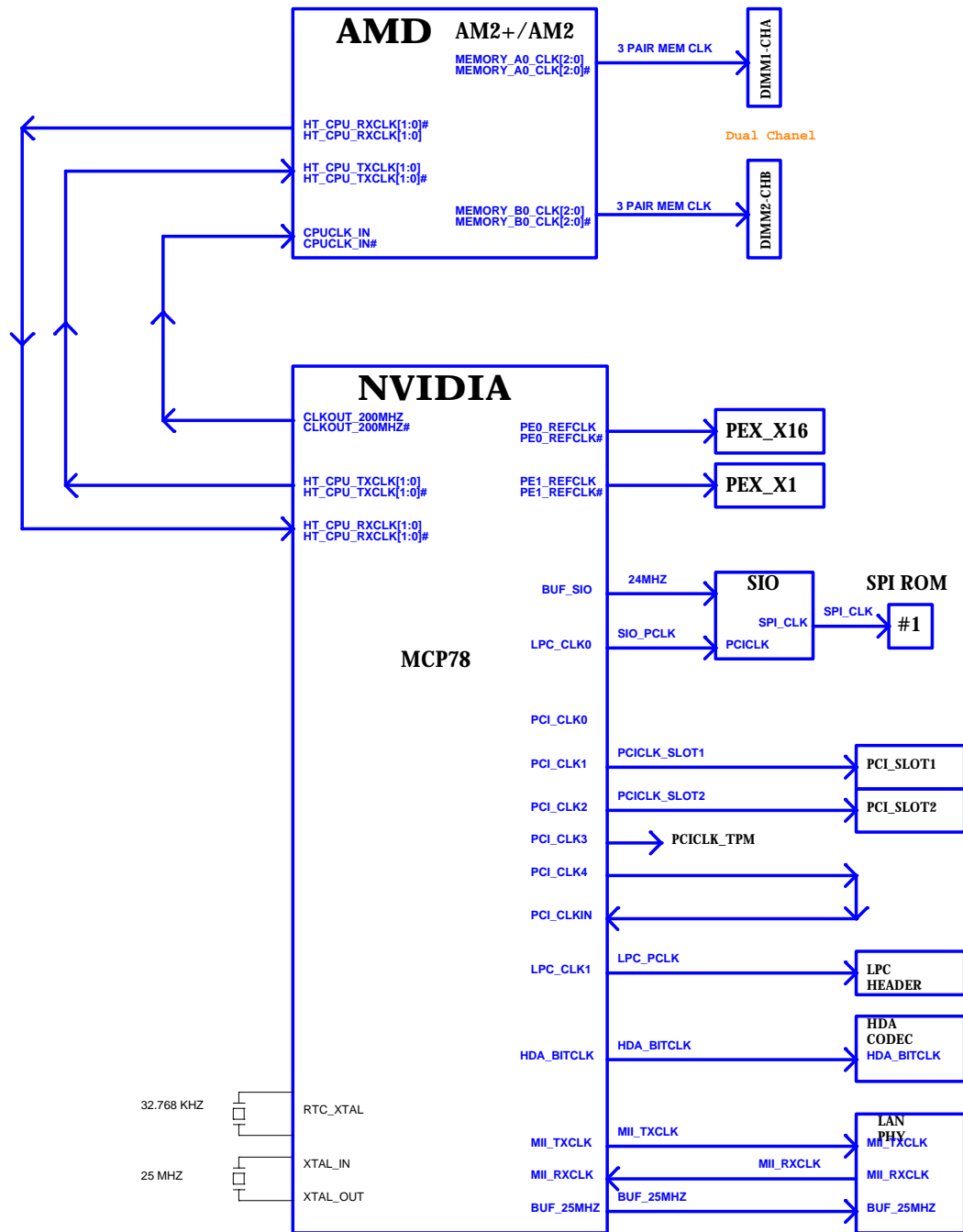
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 2	PCI_INT#X PCI_INT#Y PCI_INT#Z PCI_INT#W	PCI_REQ4# PCI_GNT4#	AD25	PCI_CLKSLOT1 (PCICLK1)
PCI Slot 1	PCI_INT#W PCI_INT#X PCI_INT#Y PCI_INT#Z	PCI_REQ3# PCI_GNT3#	AD24	PCI_CLKSLOT2 (PCICLK2)
IEEE1394				PCIE2_CLK /PCIE2_CLK#
TPM				PCICLK_TPM (PCICLK3)
Chipset				PCI_CLKIN (PCICLK4)
LPC				LPC_PCLK
SIO				SIO_PCLK

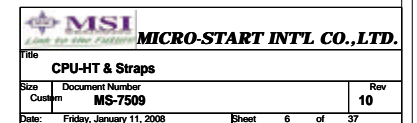
PCI RESET DEVICE

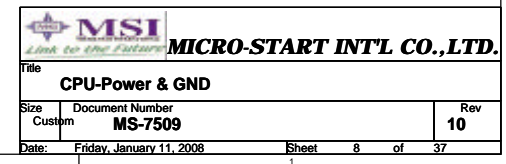
MCP78	
Signals	Target
PCI_RESET0*	PCISLOT1
PCI_RESET1*	PCISLOT2
PCI_RESET2*	MS6
PCI_RESET3*	1394
LPC_RESET*	LPC/SIO

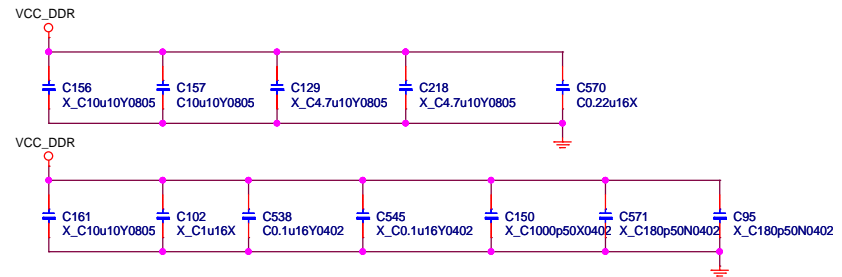
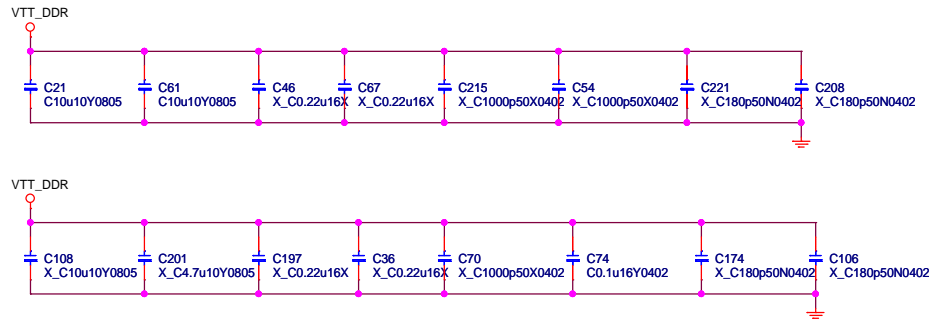
CPU VID TABLE

VID	VOLTAGE
00000	1.5500V
00001	1.5250V
00010	1.5000V
00011	1.4750V
00100	1.4500V
00101	1.4250V
00110	1.4000V
00111	1.3750V
01000	1.3500V
01001	1.3250V
01010	1.3000V
01011	1.2750V
01100	1.2500V
01101	1.2250V
01110	1.2000V
01111	1.1750V
10000	1.1500V
10001	1.1250V
10010	1.1000V
10011	1.0750V
10100	1.0500V
10101	1.0250V
10110	1.0000V
10111	0.9750V
11000	0.9500V
11001	0.9250V
11010	0.9000V
11011	0.8750V
11100	0.8500V
11101	0.8250V
11110	0.8000V
11111	0.7750V

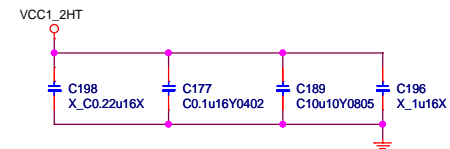
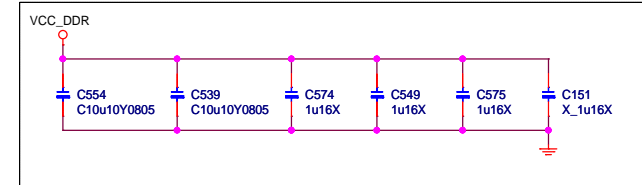




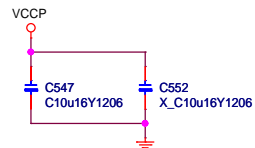
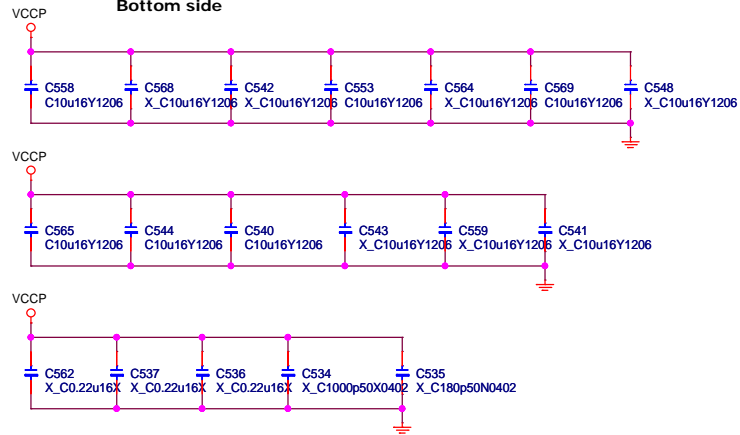


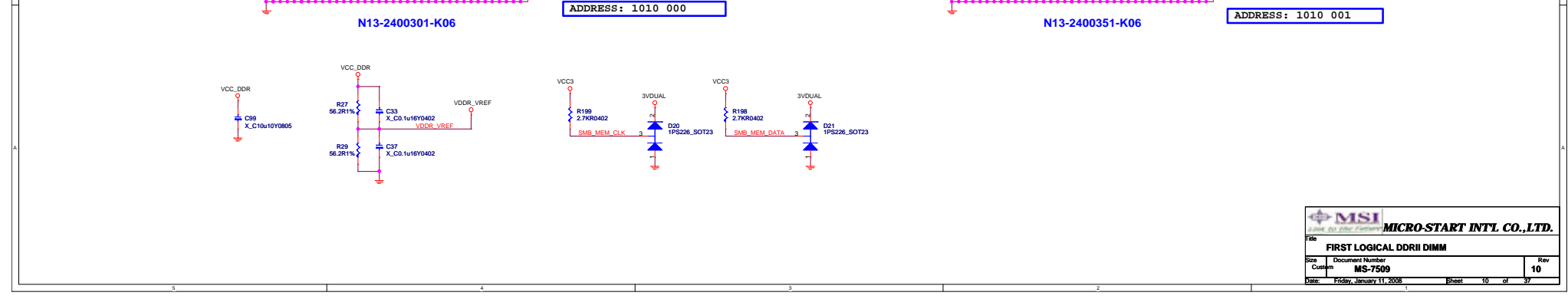
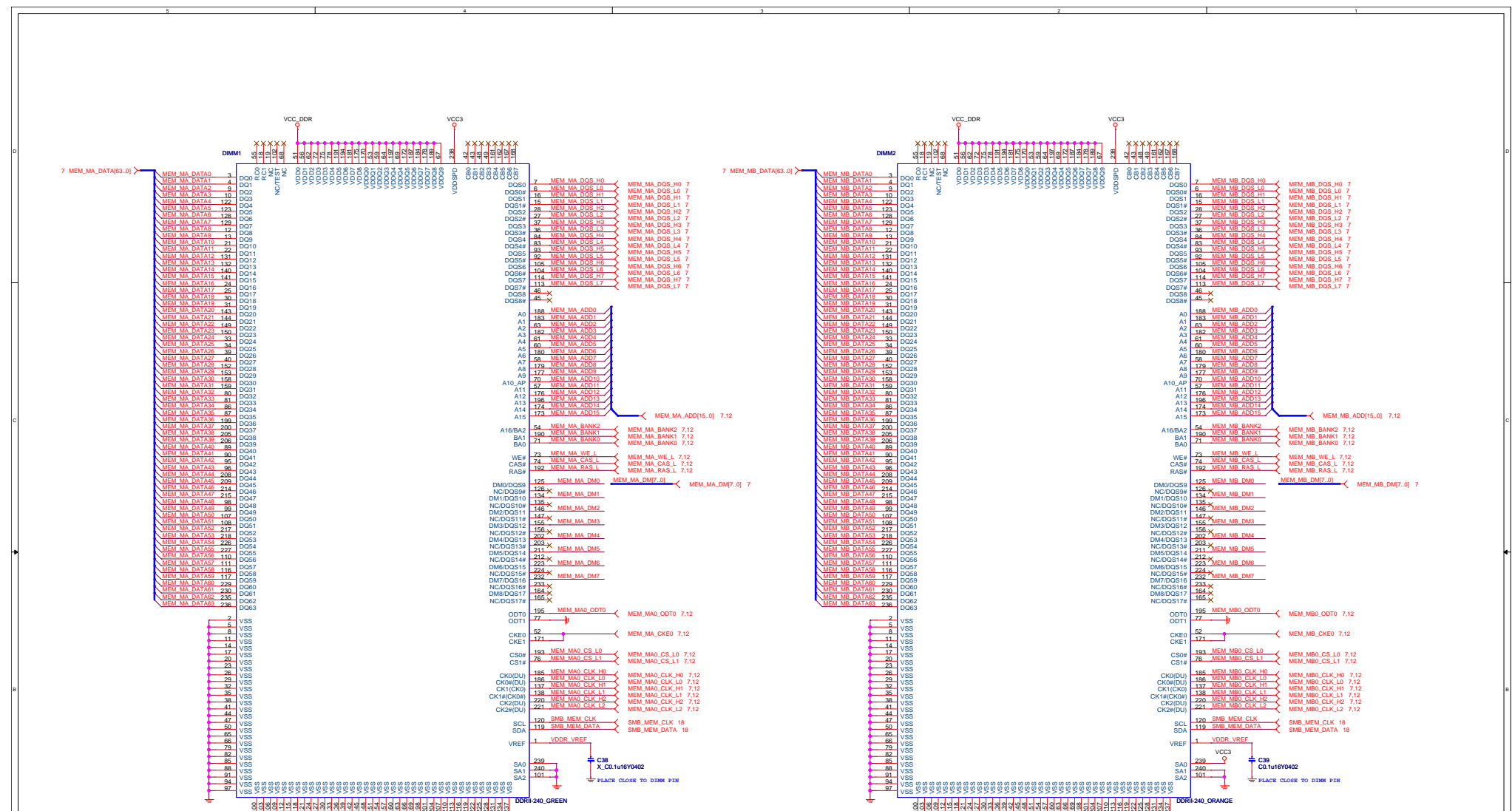


Bottom side

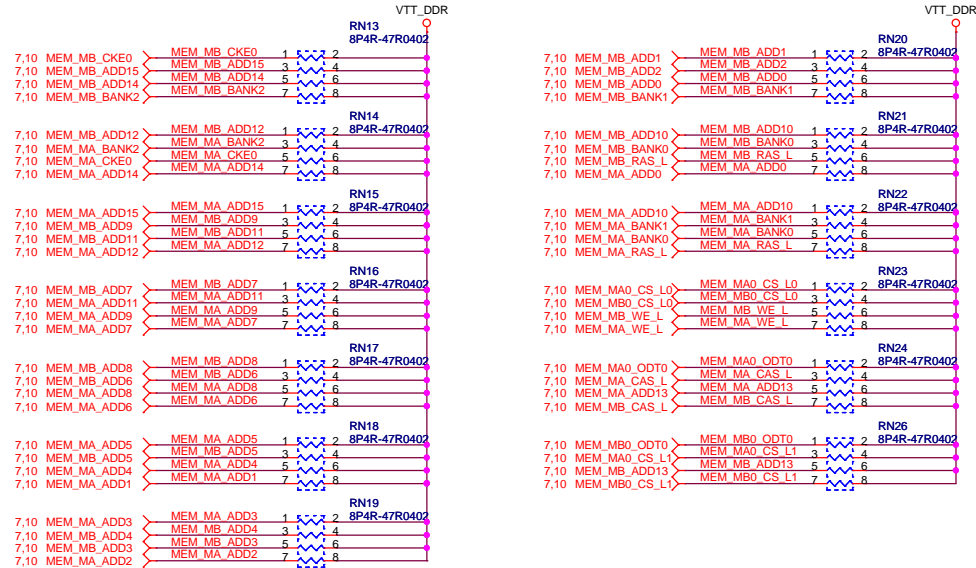


Bottom side

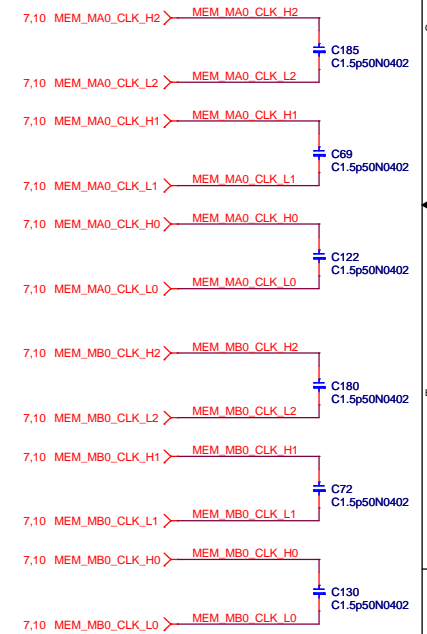
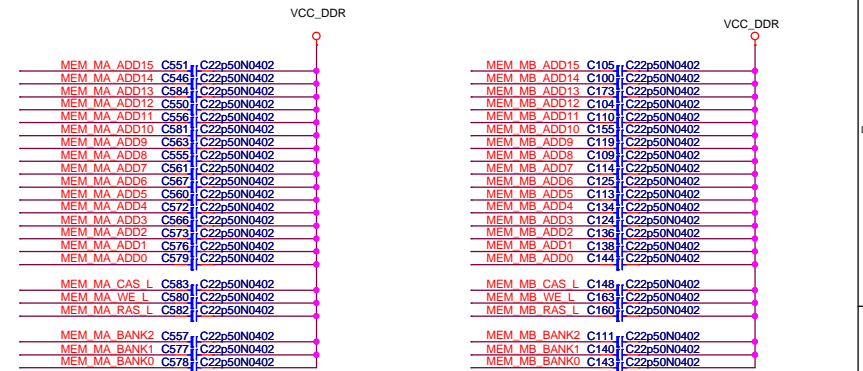




RTT:Place Behind DIMMs



Place Between Processor and DIMMs



MCP68 HyperTransport Receive

Connect directly to CPU HT Transmit Data Bus

CADOP[0..7] P/I N CADOP[8..15] P/I N
CTLPO P/I N CTLPI P/I N
CLKOP P/I N CLKOP P/I N

Breakout (<700 mil):

Route signal at nominal impedance and 1x trace width spacing.

After Breakout:

Route signal at the impedance specified in AMD Processor Motherboard Design Guide and 4x trace width spacing to other signals.

Match pairs to 25 mil.

All signal lengths must match to within 60 mil of

Minimum Length: 1" (150ps)

Maximum Length: 12" (1800ps) for trace ≥ 5mil and 8" (1200ps) for trace = 4mil

MCP68 HyperTransport Transmit

Connect directly to CPU HT Transmit Data Bus

CADIP[0..7] P/I N CADIP[8..15] P/I N
CTLIP P/I N CTLIP P/I N
CLKIP P/I N CLKIP P/I N

Breakout (<700 mil):

Route signal at nominal impedance and 1x trace width spacing.

After Breakout:

Route signal at the impedance specified in AMD Processor Motherboard Design Guide and 4x trace width spacing to other signals.

Match pairs to 25 mil.

All signal lengths must match to within 60 mil of

Minimum Length: 1" (150ps)

Maximum Length: 12" (1800ps) for trace ≥ 5mil and 8" (1200ps) for trace = 4mil

NF-6100-430-N-A2 (MCP61P) : B01-MCP6135-N08

NF-7050-630A-A1 (MCP68) : B01-MCP6805-N08

U14A
PBG692

MCP68
SEC 1 OF 8

6 CADOP[0..15] > CADOP[0..15]

6 CADON[0..15] > CADON[0..15]

6 CLKOP0 > CLKOP0
6 CLKON0 > CLKON0
6 CLKOP1 > CLKOP1
6 CLKON1 > CLKON1

6 CTLPO > CTLPO
6 CTLO0 > CTLO0
6 CTLPI > CTLPI
6 CTLO1 > CTLO1

VCC_DDR
R131 300R0402
VCC1.2
R150 150R1%0402 HT_MCP_COMP_VDD AB9
R338 150R1%0402 HT_MCP_COMP_GND AB8
R39, R52
Within 600 mils of MCP68

5/10/10

VCC1.2

1.2V_PLL_CPU_HT

1.2V_PLL_CPU_HT

70

1.2V_PLL_CPU_HT

+1.2V_PLL_CPU_HT

+3.3V_PLL_CPU

Solder Side

PIN AB15 MCP68 = 3.3V/MCP78=1.1V

HyperTransport Calibration

HT_MCP_COMP_VDD
HT_MCP_COMP_GND

Breakout (<500 mil):

Route signal at nominal impedance and 1x trace width spacing.

After Breakout:

Route signal at nominal impedance and 2x (or greater) trace width spacing.
Maximum Length: 600 mil.

MCP HyperTransport

HT_MCP_REQ# / -LDTSTOP
-LDT_RST# / CPU_GD

Breakout (<700 mil):

Route signal at nominal impedance and 1x trace width spacing.

After Breakout:

Route signal at nominal impedance and 2x trace width spacing.

HT_MCP_TXD0_P AH23 CADIP0
HT_MCP_TXD1_P AH22 CADIP1
HT_MCP_TXD2_P AJ21 CADIP2
HT_MCP_TXD3_P AH21 CADIP3
HT_MCP_TXD4_P AH19 CADIP4
HT_MCP_TXD5_P AH18 CADIP5
HT_MCP_TXD6_P AJ17 CADIP6
HT_MCP_TXD7_P AH17 CADIP7
HT_MCP_TXD8_P AE22 CADIP8
HT_MCP_TXD9_P AB20 CADIP9
HT_MCP_TXD10_P AC20 CADIP10
HT_MCP_TXD11_P AE20 CADIP11
HT_MCP_TXD12_P AD18 CADIP12
HT_MCP_TXD13_P AE18 CADIP13
HT_MCP_TXD14_P AB17 CADIP14
HT_MCP_TXD15_P AC16 CADIP15

HT_MCP_TXD0_N AJ23 CADIN0
HT_MCP_TXD1_N AJ22 CADIN1
HT_MCP_TXD2_N AK21 CADIN2
HT_MCP_TXD3_N AG21 CADIN3
HT_MCP_TXD4_N AJ19 CADIN4
HT_MCP_TXD5_N AJ18 CADIN5
HT_MCP_TXD6_N AK17 CADIN6
HT_MCP_TXD7_N AG17 CADIN7
HT_MCP_TXD8_N AG22 CADIN8
HT_MCP_TXD9_N AB19 CADIN9
HT_MCP_TXD10_N AD20 CADIN10
HT_MCP_TXD11_N AF20 CADIN11
HT_MCP_TXD12_N AE18 CADIN12
HT_MCP_TXD13_N AG18 CADIN13
HT_MCP_TXD14_N AB16 CADIN14
HT_MCP_TXD15_N AD16 CADIN15

HT_MCP_TX_CLK0_P AH20 CLKIP0
HT_MCP_TX_CLK0_N AG20 CLKIN0
HT_MCP_TX_CLK1_P AC18 CLKIP1
HT_MCP_TX_CLK1_N AB18 CLKIN1

HT_MCP_TXCTL0_P AH16 CTLIP0
HT_MCP_TXCTL0_N AG16 CTLO0
RESERVED AE16 CTLIP1
RESERVED AF16 CTLO1

HT_MCP_REQ# AH25 HT_MCP_REQ#
HT_MCP_STOP# AH24 LDTSTOP#
HT_MCP_RST# AG23 LDT_RST#
HT_MCP_PWRGD AG24 CPU_GD

CLKOUT_200MHZ_P AK25 CPUCLKO_H
CLKOUT_200MHZ_N AJ25 CPUCLKO_L

CPU_SBVREF AE24

CLKOUT_25MHZ AK26

CLK200_TERM_GND AJ26

MCP68/A1/PBG692

5/10/10

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

width 8 mil

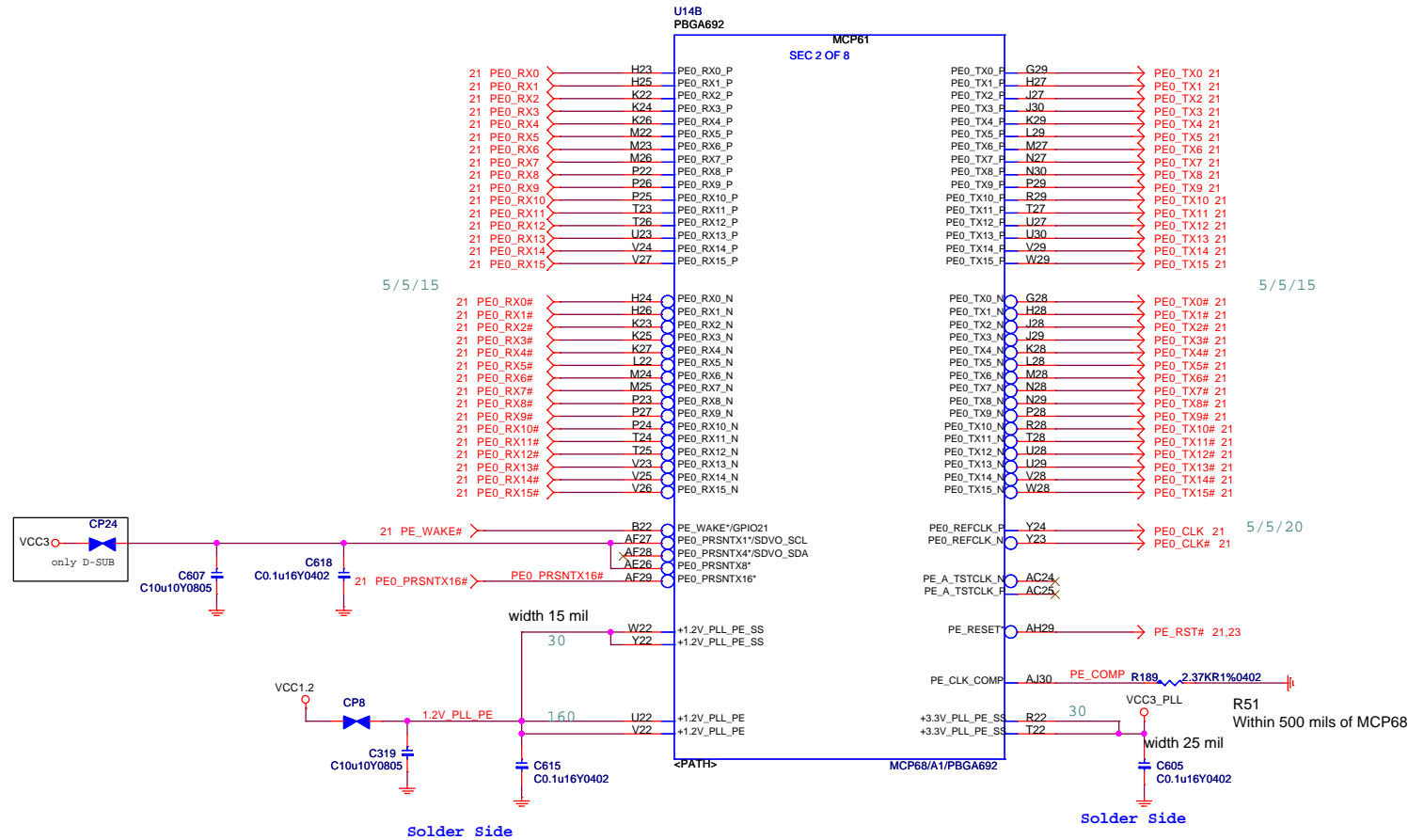


MICRO-START INTL CO.,LTD.

Title MCP68-HT

Size Custom Document Number MS-7509 Rev 10


Date: Friday, January 11, 2008 Sheet 13 of 37

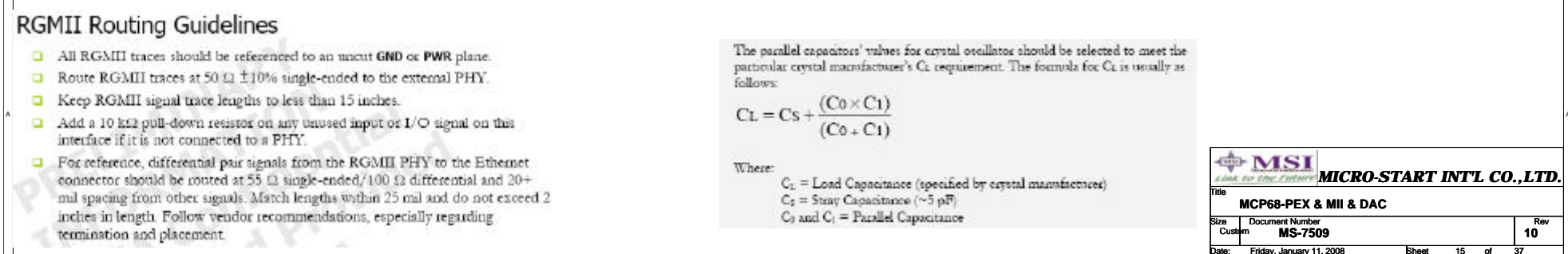


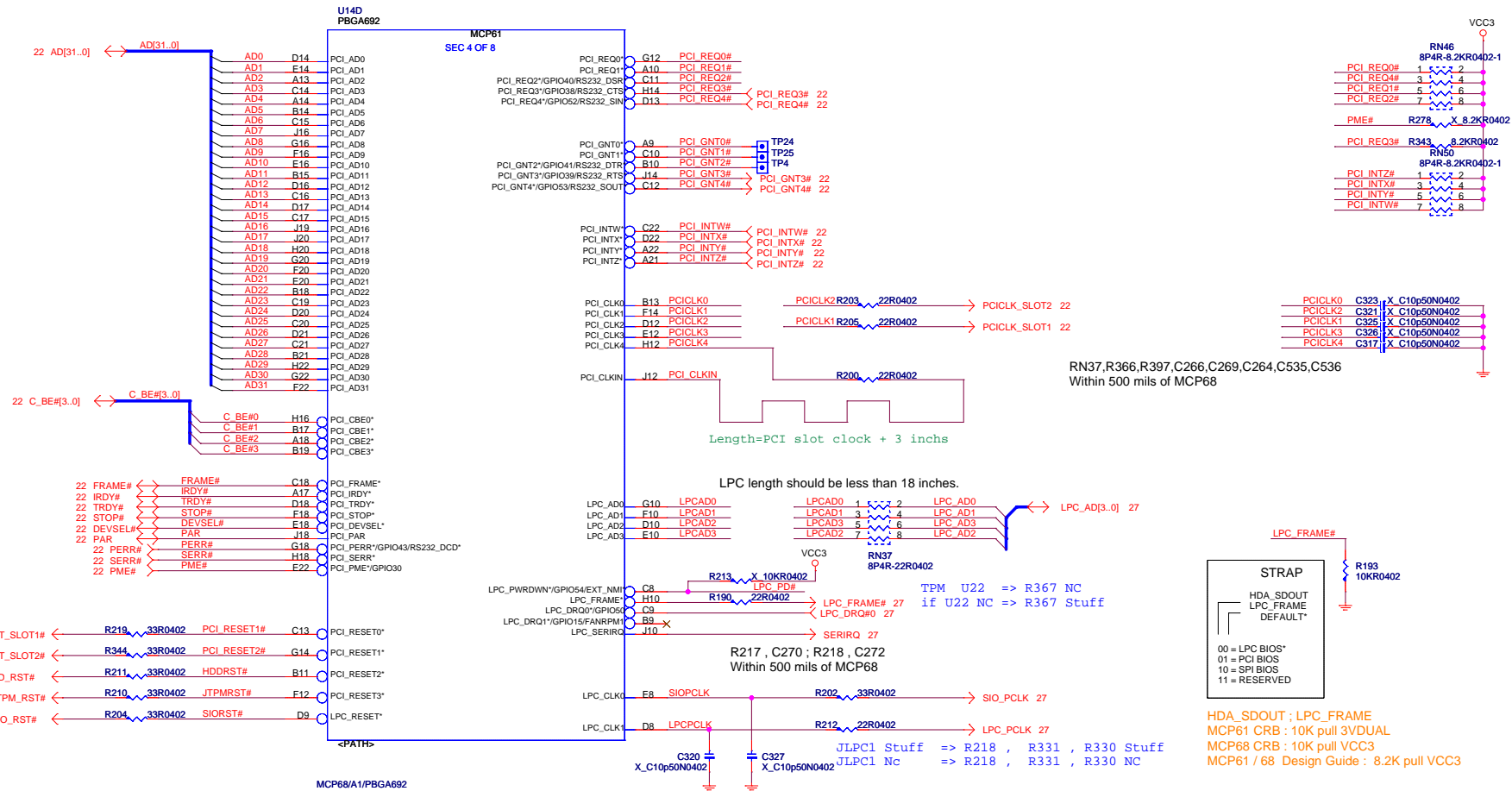
PCI Express Layout Guidelines

The PCI Express differential signal groups are very high speed, running at 2.5 Gbps. Pay special attention to routing these signals.

- Nominal impedance: the differential signal group should be routed at 60Ω $\pm 10\%$ single-ended and 100Ω $\pm 10\%$ differential.
- Maintain 5 mil length matching within each pair, and 20 mil spacing to other pairs and signals, unless otherwise specified.
- Maximum mismatch between pairs is 3,000 mil, and maximum length of any pair is 10,000 mil.
- All traces should be referenced to GND.
- There should be no more than four vias per TX trace, and no more than two vias per RX trace on the motherboard.

 MICRO-START INT'L CO.,LTD.		
Title MCP68-PEX X16		
Size Custom	Document Number MS-7509	Rev 10
Date: Friday, January 11, 2008	Sheet 14	of 37



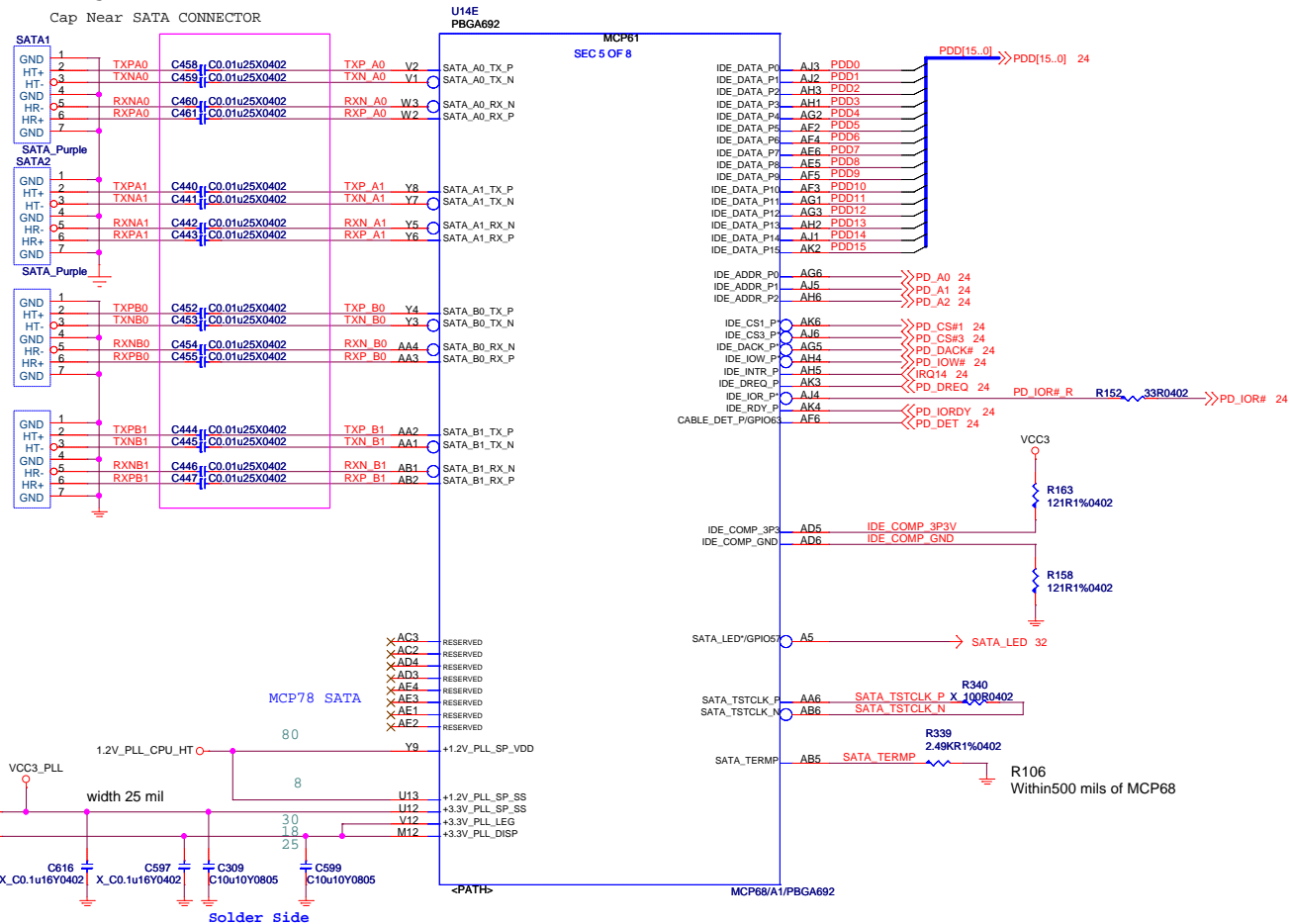


Trace lengths must be less 8 inches

Cap Near SATA CONNECTOR

N5N-07M0231-H06

MCP61P NC
MCP68 Stuff up
MCP78 Stuff up




Single-Ended Impedance

Trace Width (Based on 4-Layer Stackup)	Impedance	Interfaces
5 mil	60 Ω $\pm 10\%$	All other interfaces
7 mil	50 Ω $\pm 10\%$	RGMII, SATA
7.5 mil	45 Ω $\pm 10\%$	USB

Differential Impedance

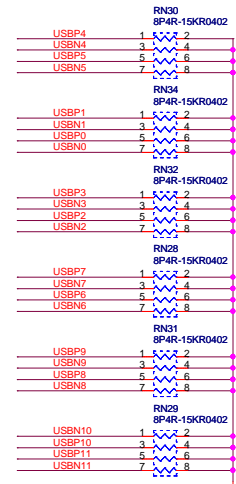
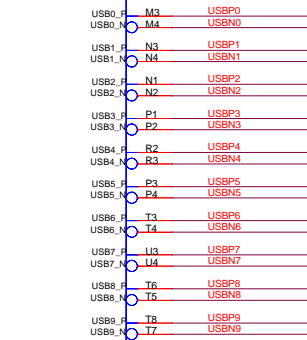
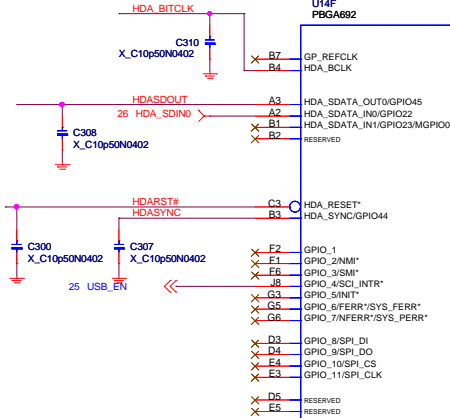
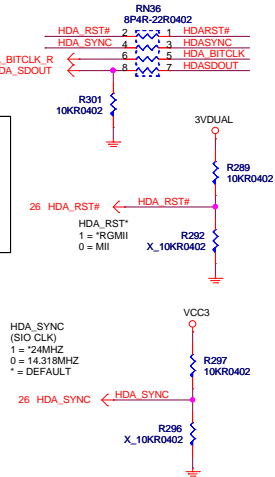
Trace Width (4-Layer Stackup)	Trace Spacing (4-Layer Stackup)	Impedance	Interfaces
5 mil	5 mil	93 Ω $\pm 10\%$	HyperTransport
5 mil	6 mil	100 Ω $\pm 10\%$	PCI Express
7 mil	12 mil	100 Ω $\pm 10\%$	SATA
7.5 mil	7.5 mil	90 Ω $\pm 10\%$	USB

 MICRO-START INT'L CO.,LTD.	
Title MCP68-SATA & IDE	
Size Custom	Document Number MS-7509
Date Friday, January 11, 2008	Rev 10
Sheet 17 of 37	

HDA_SDOUT : LPC_FRAME
MCP61 CRB : 10K pull 3VDUAL
MCP68 CRB : 10K pull VCC3
MCP61 / 68 Design Guide : 8.2K pull VCC3

STRAP
HDA_SDOUT
LPC_FRAME
DEFAULT*

00 = LPC BIOS*
01 = PCI BIOS
10 = SPI BIOS
11 = RESERVED



RN30 8P4R-15KR0402
USBP4 1 2
USBN4 3 4
USBP5 5 6
USBN5 7 8
RN34 8P4R-15KR0402
USBP1 1 2
USBN1 3 4
USBP0 5 6
USBN0 7 8
RN32 8P4R-15KR0402
USBP3 1 2
USBN3 3 4
USBP2 5 6
USBN2 7 8
RN28 8P4R-15KR0402
USBP7 1 2
USBN7 3 4
USBP6 5 6
USBN6 7 8
RN31 8P4R-15KR0402
USBP9 1 2
USBN9 3 4
USBP8 5 6
USBN8 7 8
RN29 8P4R-15KR0402
USBP10 1 2
USBN10 3 4
USBP11 5 6
USBN11 7 8

Close to MCP61
R341 8450HM
MCP78 DA-03365-001_v06

C281 C0.01u25X0402
C272 C0.01u25X0402
C590 C0.01u25X0402
C589 C0.01u25X0402
R165 MCP68
1Meg Ohm.
CRB 49.9KOhm.

MCP68 CRB SIO_OVT# OUTPUT
USED FOR EXT_SMI*

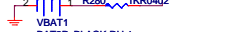
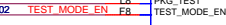
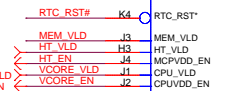
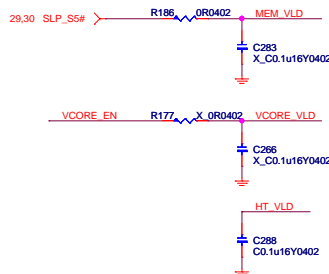
Y6 NC => Stuff R383, R564
NC R562, R563 C509, C526
Y6 Stuff => NC R383, R564
Stuff R562, R563 C509, C526

R207,C263,R383,C559
Within 500 mils of MCP68

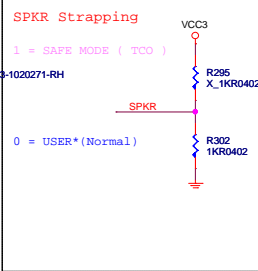
5/10/10

for NV R453, R454 Stuff
for SIO R453, R454 NC

POWER SEQUENCE



CMOS CLEAR JUMPER	
JBAT1	Clear CMOS
1-2	Normal
2-3	Clear CMOS



SPKR
Boot mode
select
0: User Mode Boot Init table (TCO
timer enabled)
1: Safe Mode Boot Init table (TCO
timer disabled)

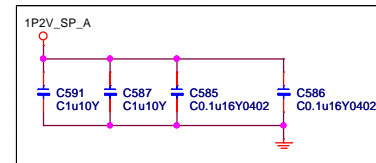
Selects between a USER table and a
SAFE table for boot initialization
parameters.
Note: When booting the SAFE table,
it is assumed that the boot values are
valid, so the automatic recovery logic
is disabled (TCO timer does not
reboot the system).

MCP68

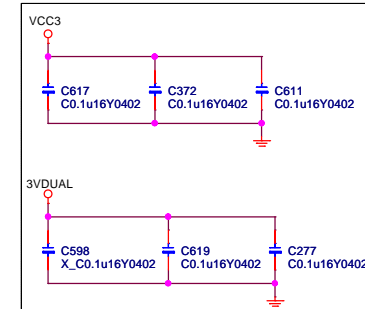
Preliminary Thermal Properties and Recommended Limits

Parameter	Value	Notes
Design ambient	43 °C	AMD max internal case temperature for CPU
Minimum Case to Ambient Solution	4.6 C/W	Assume 90% to heat sink and 10% to printed circuit board
TDP Max	13 W	Thermal Design Power (TDP) based on worst case process
Tcase Max	110 °C	Measured top center of chip without heat sink

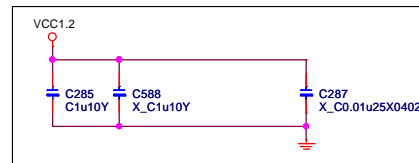
BACK SIDE



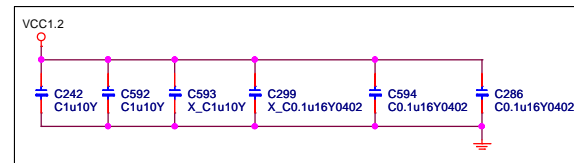
BACK SIDE



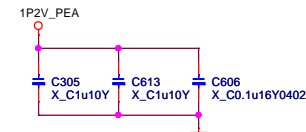
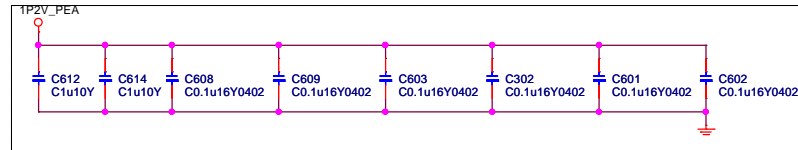
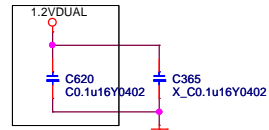
PLACE ON BACK SIDE
CENTER OF MCP68



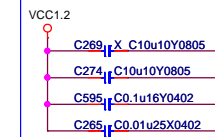
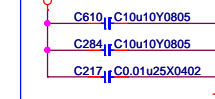
BACK SIDE



BACK SIDE

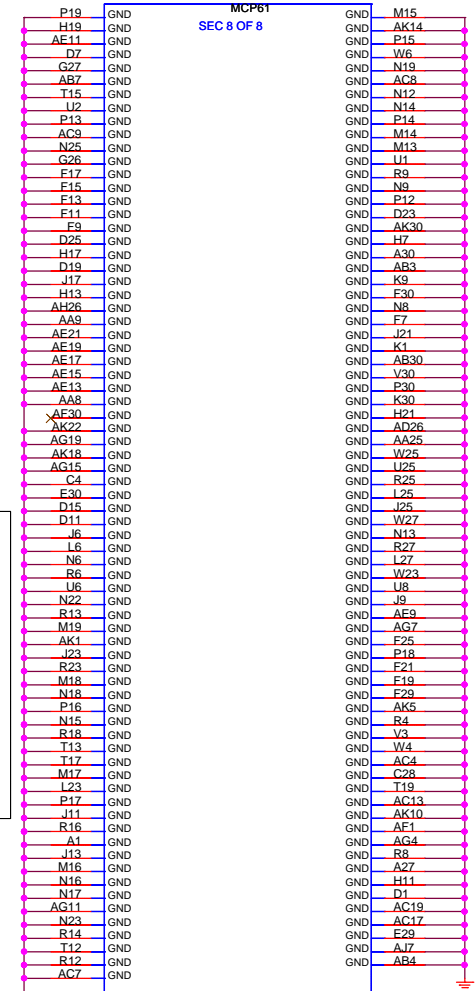


Place close to Q34

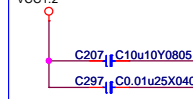


U14H
PBG692

MCP61
SEC 8 OF 8

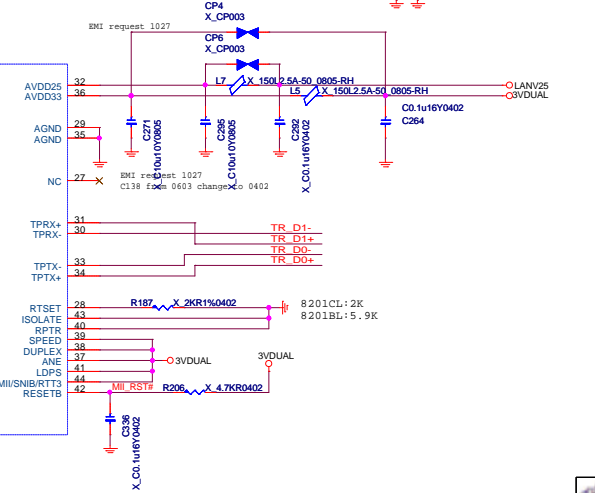
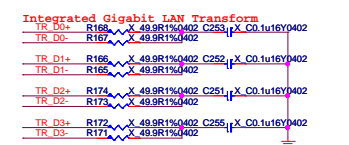
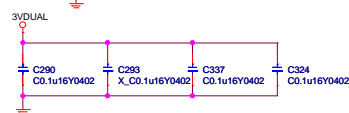
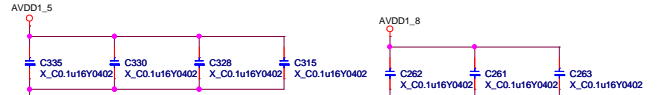
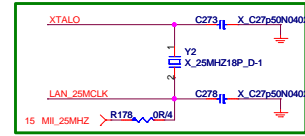
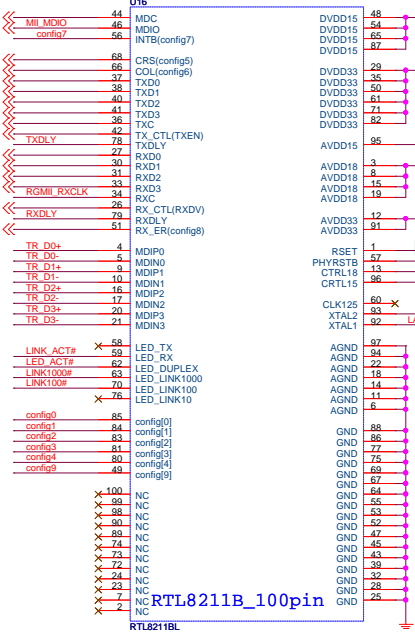
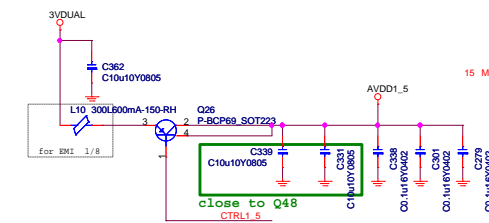
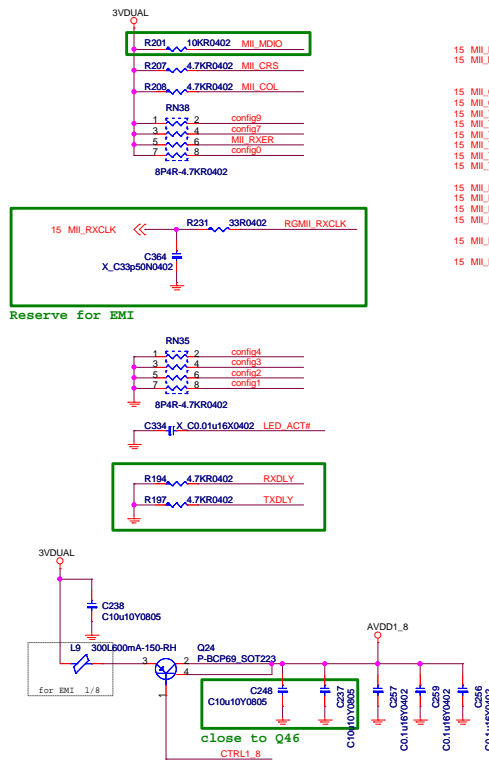


Place close to Q22

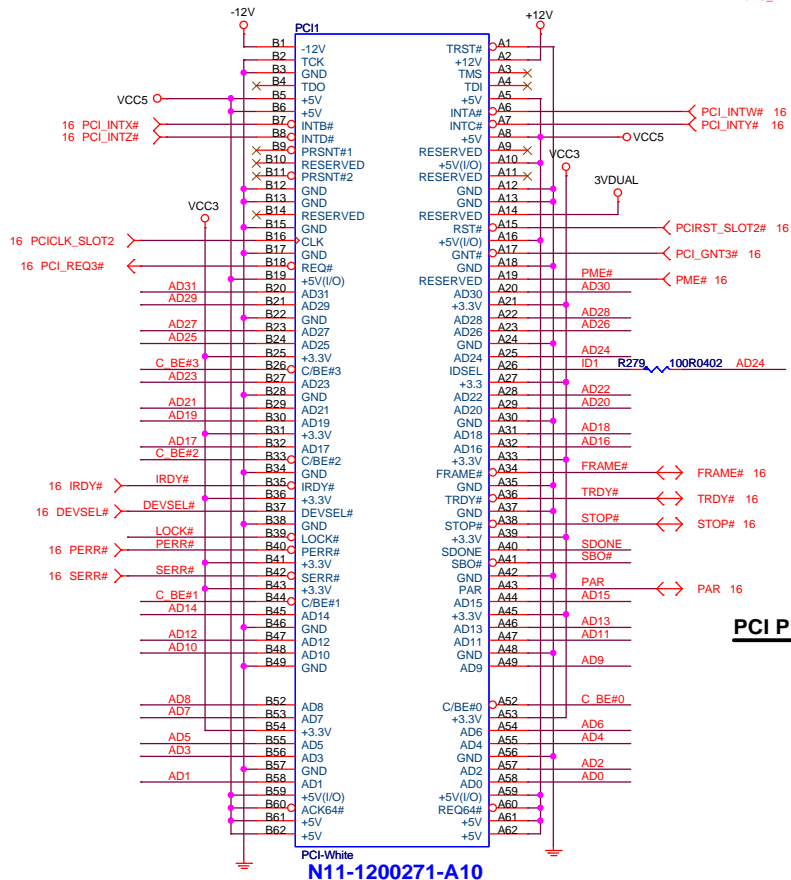


MICRO-START INT'L CO.,LTD.

Title MCP68-Power & GND			Rev 10
Size Custom	Document Number MS-7509		
Date: Friday, January 11, 2008	Sheet 19	of 37	

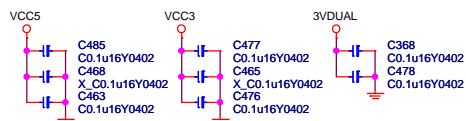


PCI SLOT 1 (PCI VER: 2.3 COMPLY)



MCP61P	MCP68
IDSEL = AD24	IDSEL = AD24
PCI_REQ2# PCI_GNT2#	PCI_REQ3# P
PCI_INTW#	PCI_INTW#
Device # 7	Device # 8

PCI SLOT DECOUPLING CAPACITORS



MCP61 IDSEL, INT, and REQ/GNT

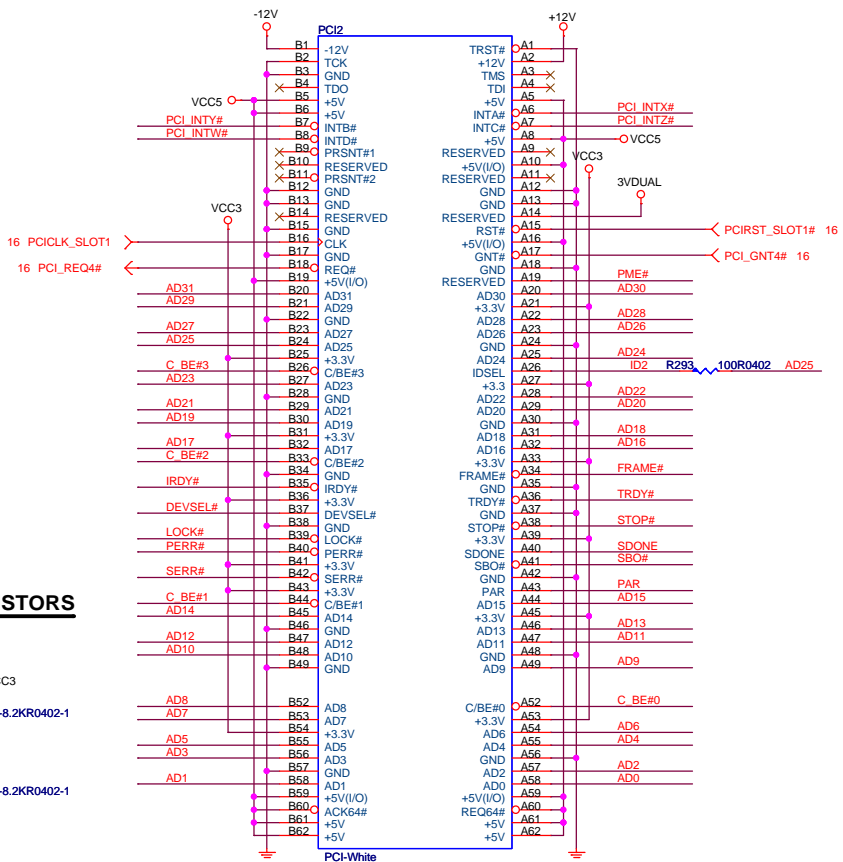
Slot	IDSEL	Slot INTA#	Slot INTB#	Slot INTC#	Slot INTD#	REQ/GNT	Device #
1	PCI_A025	INTA#	INTB#	INTC#	INTD#	4	5
2	PCI_A025	INTA#	INTC#	INTD#	INTB#	1	0
3	PCI_A024	INTA#	INTB#	INTD#	INTC#	2	7
4	PCI_A023	INTA#	INTB#	INTD#	INTC#	1	6
5	PCI_A022	INTA#	INTB#	INTC#	INTD#	0	5

MCP68 IDSEL, INT, and REQ/GNT

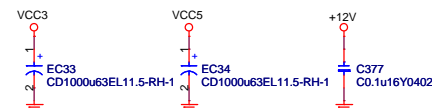
Slot	IDSEL	Slot INTA#	Slot INT#
1	PCI_A025	INTx#	INT#
2	PCI_A024	INTx#	INT#
3	PCI_A023	INTx#	INT#
4	PCI_A022	INTx#	INT#
5	PCI_A021	INTx#	INT#

REQ/GINT	Device #
4	9
3	8
2	7
1	6
0	5

PCI SLOT 2 (PCI VER: 2.3 COMPLY)

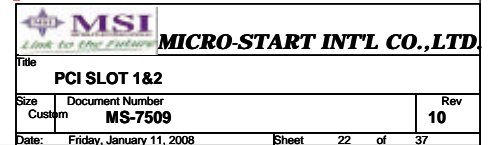


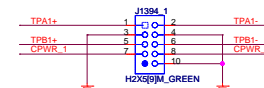
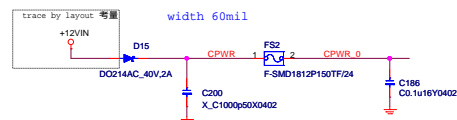
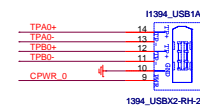
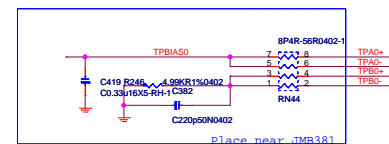
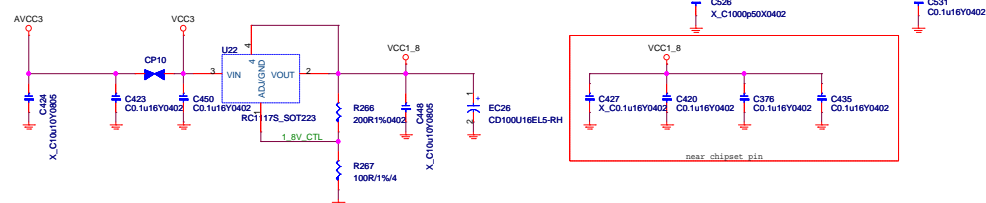
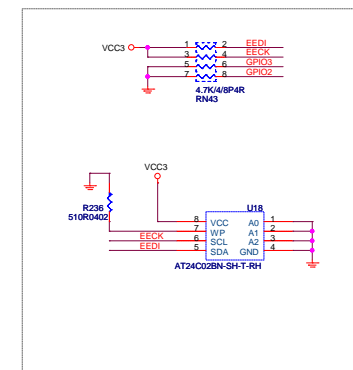
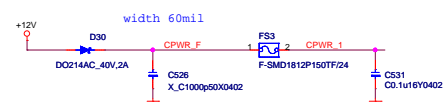
MCP61P	MCP68	SDONE SBO#
IDSEL = AD25	IDSEL = AD25	
PCI_REQ3# PCI_GNT3#	PCI_REQ4# PCI_GNT4#	
PCI_INTX#	PCI_INTX#	
Device # 8	Device # 9	



SDONE R264 X 0R0402
SBO# R265 X 0R0402

SMBCLK 18,21,29,31
SMBDATA 18,21,29,31



Rear 1394 port[illegible]

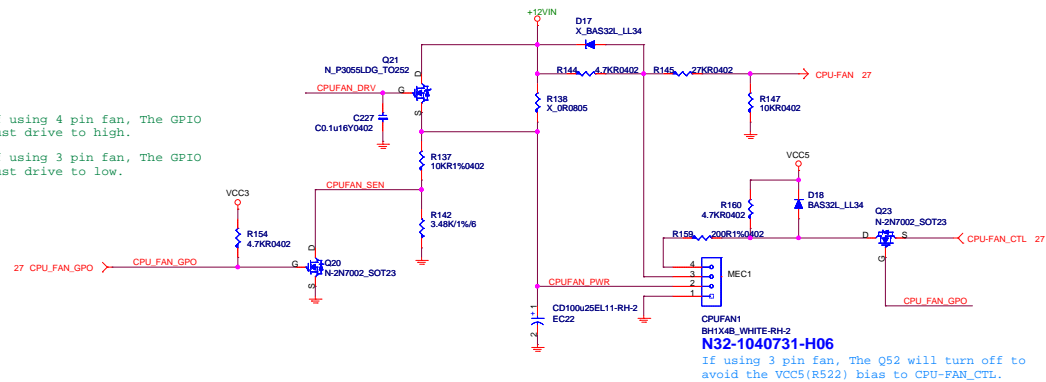
The schematic diagram illustrates the ATmega328P microcontroller with the following connections:

- VCC Connections:**
 - VCC5 is connected to pin 1 (VCC) and pin 20 (VCC).
 - VCC3 is connected to pin 3 (VCC).
- GND Connections:**
 - GND is connected to pin 14 (GND) and pin 28 (GND).
- Resistor Connections:**
 - R220 (10K) is connected between VCC5 and pin 18 (X_510R0402).
 - R156 (8.2K) is connected between VCC3 and pin 14 (X_8.2KR0402).
 - R155 (10K) is connected between VCC5 and pin 15 (IR014).
 - R160 (6.6K) is connected between VCC5 and pin 16 (PD_DREQ).
 - R164 (4.7K) is connected between VCC5 and pin 17 (PD_IOWR).
 - R149 (15K) is connected between VCC5 and pin 18 (PD_DET).
- LED Connections:**
 - IR014 is connected to pin 15.
 - IR014 is connected to pin 16.
 - IR014 is connected to pin 17.
 - IR014 is connected to pin 18.
 - IR014 is connected to pin 19.
 - IR014 is connected to pin 20.
 - IR014 is connected to pin 21.
 - IR014 is connected to pin 22.
 - IR014 is connected to pin 23.
 - IR014 is connected to pin 24.
 - IR014 is connected to pin 25.
 - IR014 is connected to pin 26.
 - IR014 is connected to pin 27.
 - IR014 is connected to pin 28.
 - IR014 is connected to pin 29.
 - IR014 is connected to pin 30.
 - IR014 is connected to pin 31.
 - IR014 is connected to pin 32.
 - IR014 is connected to pin 33.
 - IR014 is connected to pin 34.
 - IR014 is connected to pin 35.
 - IR014 is connected to pin 36.
 - IR014 is connected to pin 37.
 - IR014 is connected to pin 38.
 - IR014 is connected to pin 39.
 - IR014 is connected to pin 40.
- Other Connections:**
 - PD07 is connected to pin 1.
 - PD08 is connected to pin 2.
 - PD09 is connected to pin 3.
 - PD10 is connected to pin 4.
 - PD11 is connected to pin 5.
 - PD12 is connected to pin 6.
 - PD13 is connected to pin 7.
 - PD14 is connected to pin 8.
 - PD15 is connected to pin 9.
 - PD16 is connected to pin 10.
 - PD17 is connected to pin 11.
 - PD18 is connected to pin 12.
 - PD19 is connected to pin 13.
 - PD20 is connected to pin 14.
 - PD21 is connected to pin 15.
 - PD22 is connected to pin 16.
 - PD23 is connected to pin 17.
 - PD24 is connected to pin 18.
 - PD25 is connected to pin 19.
 - PD26 is connected to pin 20.
 - PD27 is connected to pin 21.
 - PD28 is connected to pin 22.
 - PD29 is connected to pin 23.
 - PD30 is connected to pin 24.
 - PD31 is connected to pin 25.
 - PD32 is connected to pin 26.
 - PD33 is connected to pin 27.
 - PD34 is connected to pin 28.
 - PD35 is connected to pin 29.
 - PD36 is connected to pin 30.
 - PD37 is connected to pin 31.
 - PD38 is connected to pin 32.
 - PD39 is connected to pin 33.
 - PD40 is connected to pin 34.
 - PD41 is connected to pin 35.
 - PD42 is connected to pin 36.
 - PD43 is connected to pin 37.
 - PD44 is connected to pin 38.
 - PD45 is connected to pin 39.
 - PD46 is connected to pin 40.

[illegible][illegible]

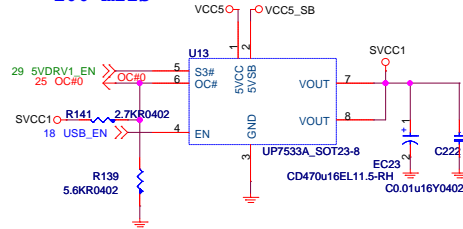
```
using 4 pin fan,
st drive to high.

using 3 pin fan,
st drive to low.
```

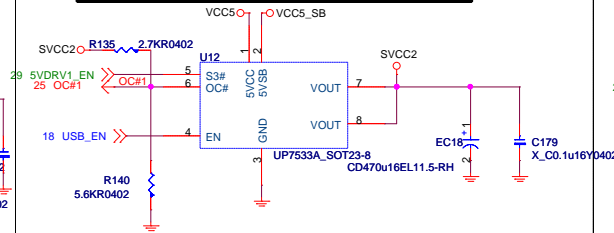


POWER CIRCUIT FOR USB PORT 0,1

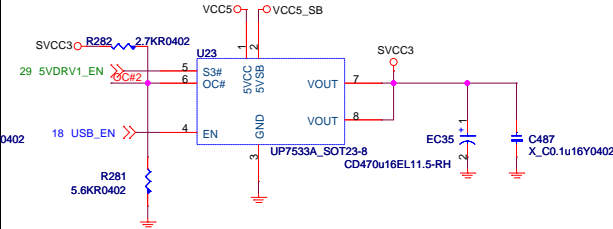
100 mils



POWER CIRCUIT FOR USB PORT 2,3

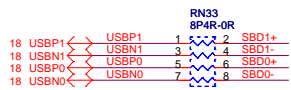


POWER CIRCUIT FOR USB PORT 4,5

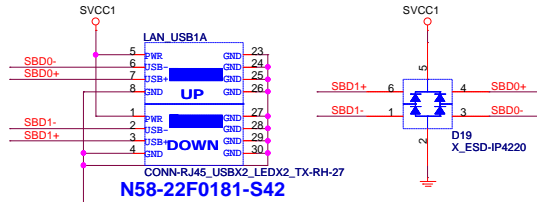


REAR PANEL USB CONNECTOR FOR USB PORT 0,1

Trace lengths must be less 12 inches



Match pairs to 50 mil.

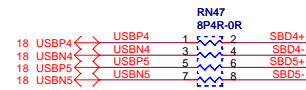


NEAR USB CONNECTOR

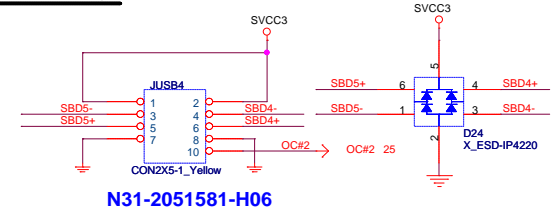
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 5 inches



Match pairs to 50 mil.

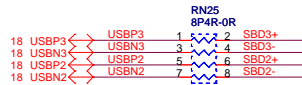


NEAR USB CONNECTOR

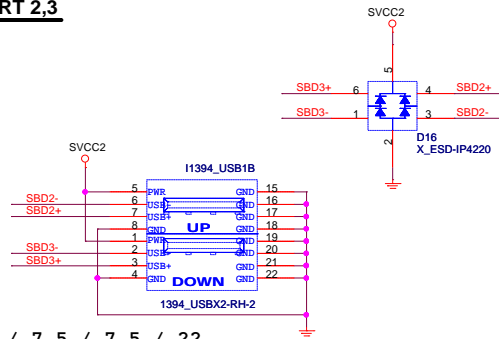
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

REAR PANEL USB CONNECTOR FOR USB PORT 2,3

Trace lengths must be less 12 inches



Match pairs to 50 mil.

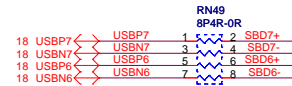


NEAR USB CONNECTOR

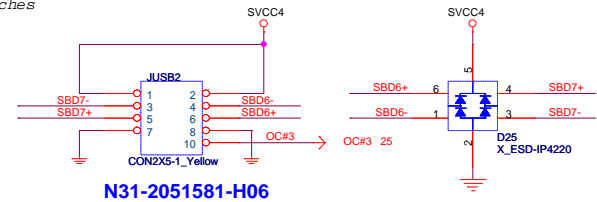
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



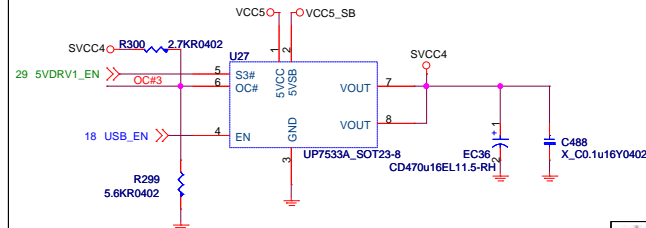
Match pairs to 50 mil.




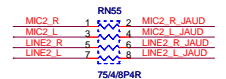
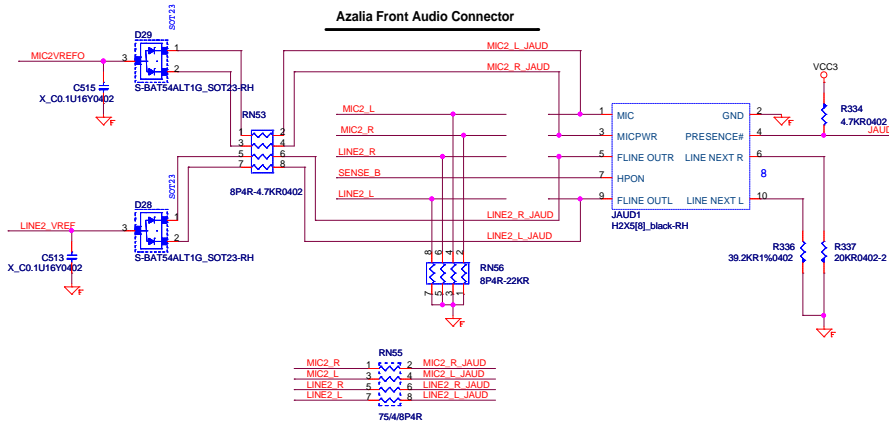
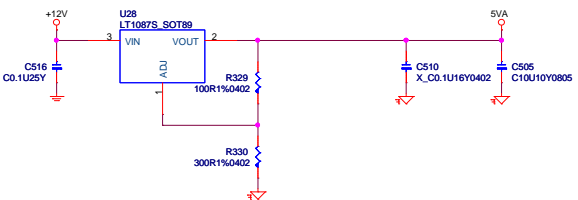
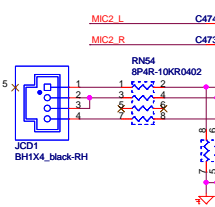
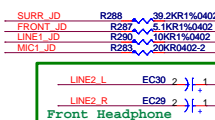
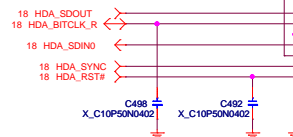
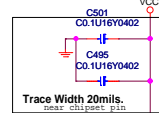
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

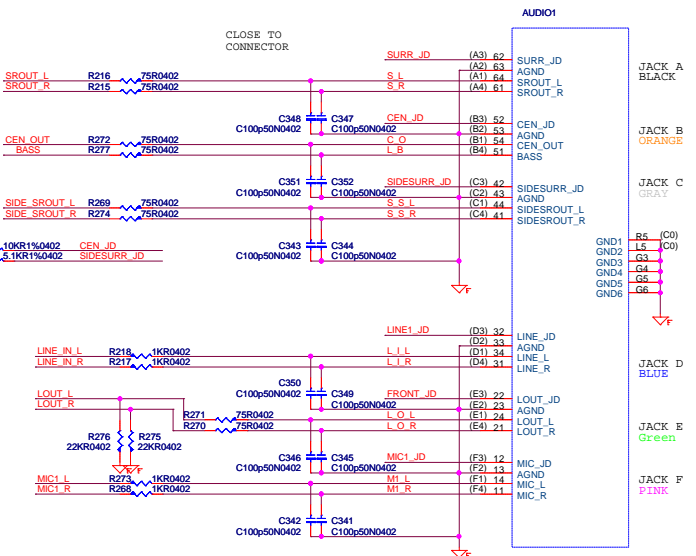
POWER CIRCUIT FOR USB PORT 6,7



 MICRO-START INT'L CO.,LTD.			
Title			
USB CONNECTOR			
Size	Document Number	Rev	
Custom	MS-7509	10	
Date:	Friday, January 11, 2008	Sheet	25 of 37

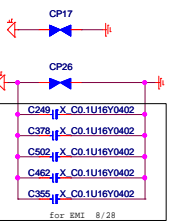
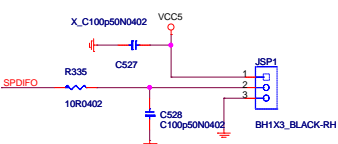


Rear audio jack

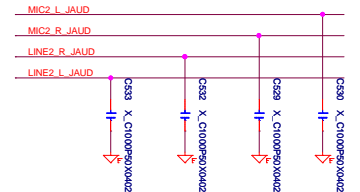


JACK-AUDIOX2X3-26P-RH-3
The N54-13P0171-542 is for 3port audio
The N54-26P0201-542 is for 6port audio

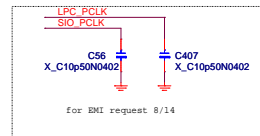
SPDIF OUT



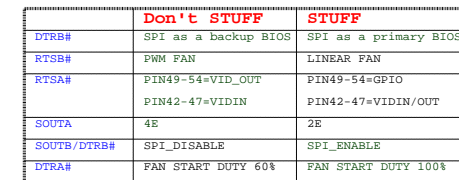
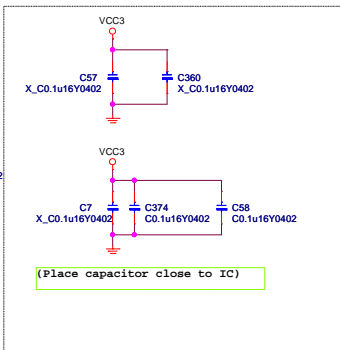
For EMI



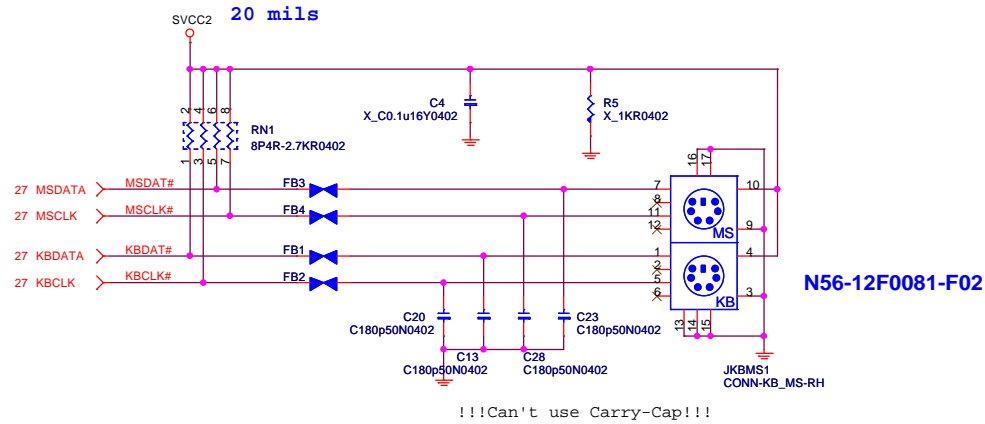
LPC length should be less than 18 inches.



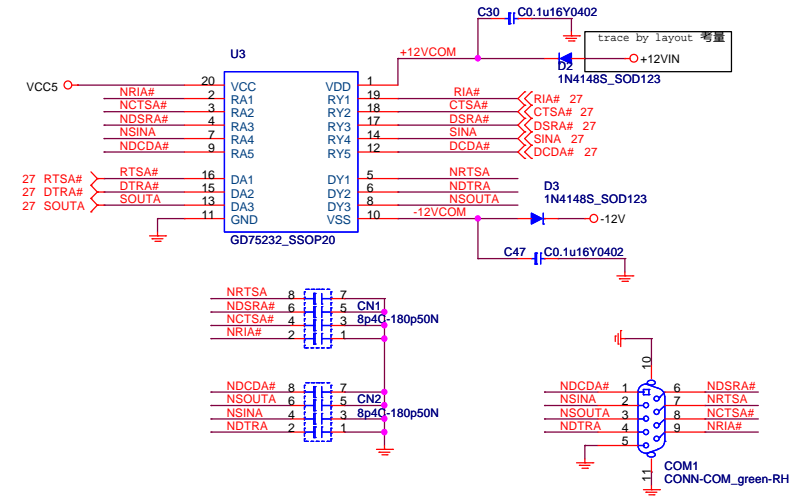
Pin configuration diagram for the HX2710JM-2PITCH_BLACK-RH package. The package is shown with pins 1 through 14. Pin 1 is labeled '16 LPC_PCLK' and '16 JTPM_RST#'. Pin 2 is labeled 'JTPM_RST#'. Pin 3 is labeled 'LPC_ADO'. Pin 4 is labeled 'LPC_ADI'. Pin 5 is labeled 'LPC_ADI'. Pin 6 is labeled 'LPC_ADI'. Pin 7 is labeled 'LPC_ADI'. Pin 8 is labeled 'LPC_ADI'. Pin 9 is labeled 'LPC_ADI'. Pin 10 is labeled 'LPC_ADI'. Pin 11 is labeled 'LPC_ADI'. Pin 12 is labeled 'LPC_ADI'. Pin 13 is labeled 'LPC_ADI'. Pin 14 is labeled 'LPC_ADI'. The package is connected to a 3V3V supply and a SERIRQ line. The package is labeled 'HX2710JM-2PITCH_BLACK-RH'.

[illegible]

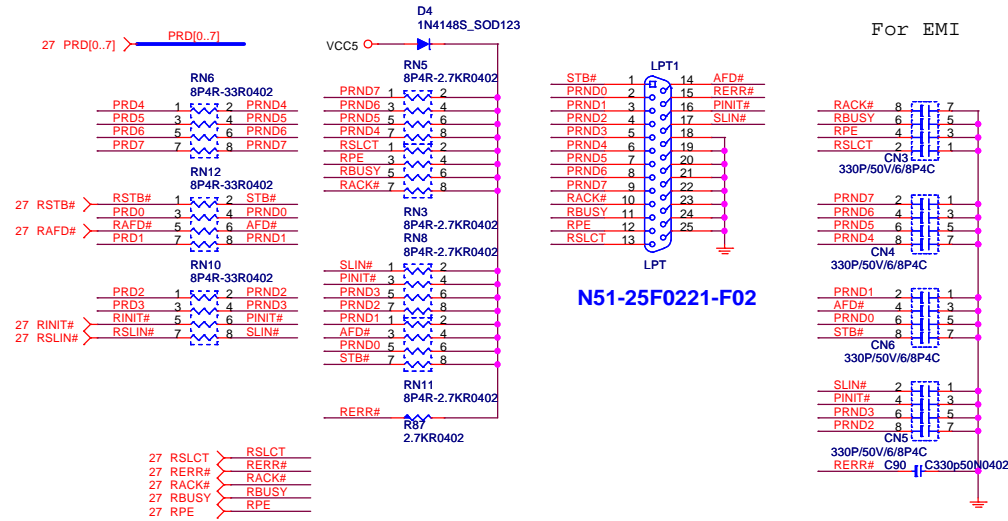
PS2 KEYBOARD & MOUSE CONNECTOR



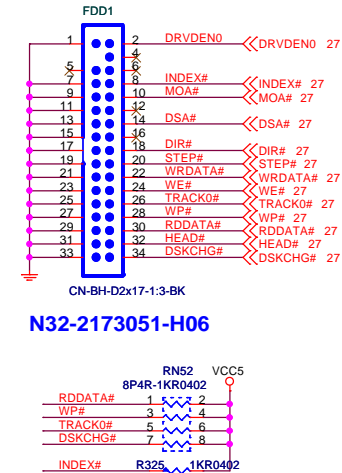
SERIAL PORT 1



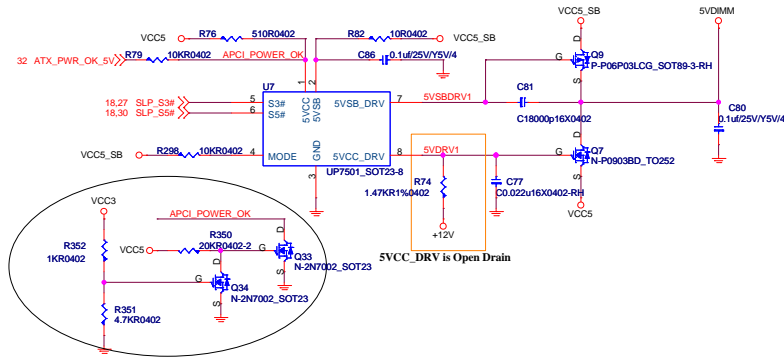
PARALLAL PORT



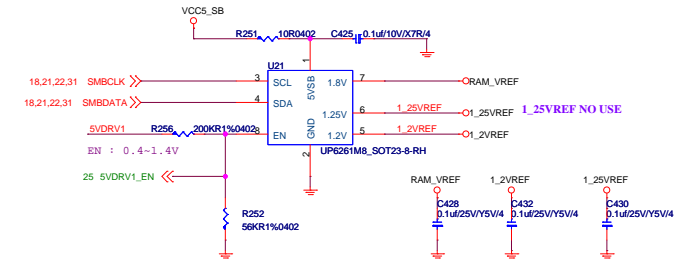
FLOPPY CONN BOLCK



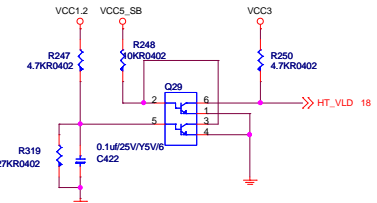
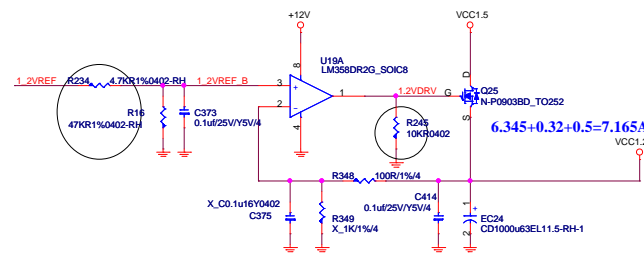
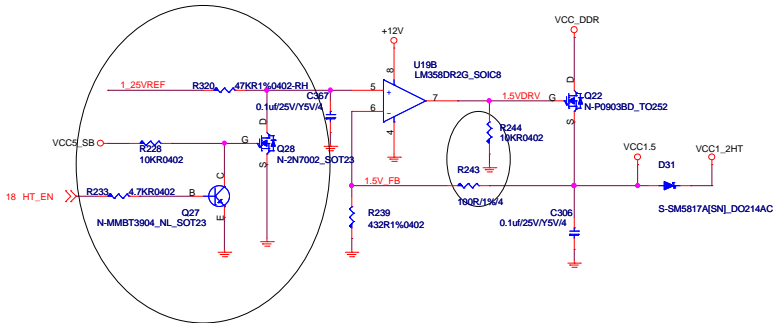
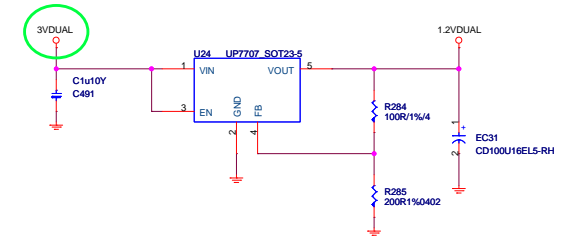
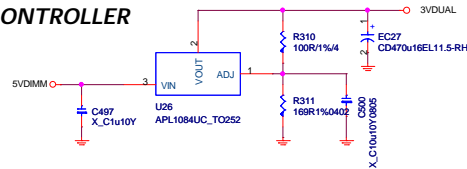
5VDIMM FOR DDR



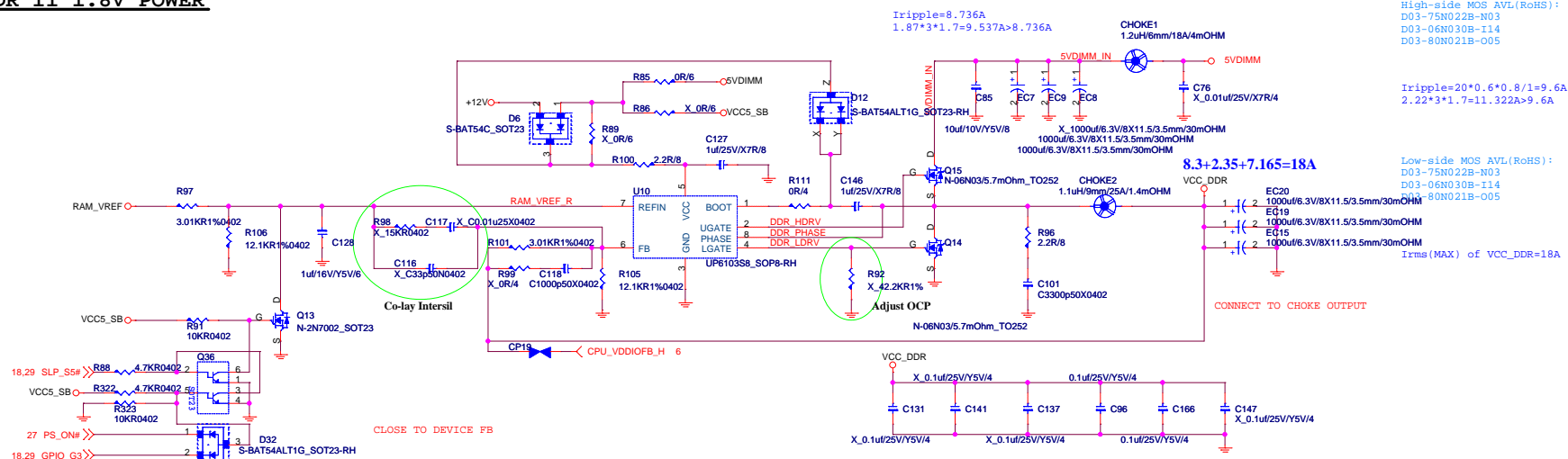
	S0	S3	S4	S5
DUAL_CTRL	X	X	0 1 1	0 1 1
5VSBDRV1	1	0	1 0 0	1 0 0
5VDRV1	1	0	0 0 0	0 0 0
5VSBDRV2	X	0	1 0 0	1 0 0
USB_EN	1	1	X 1 0	X 1 0
5VDIMM	Y	Y	N Y Y	N Y Y
USB power	Y	Y	N Y N	N Y N



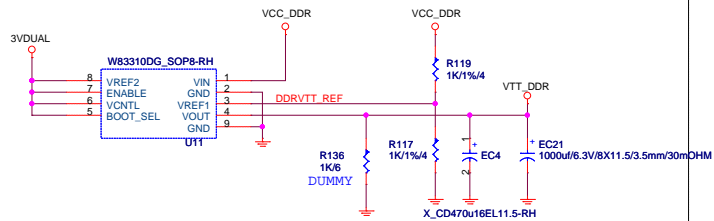
3VDUAL CONTROLLER



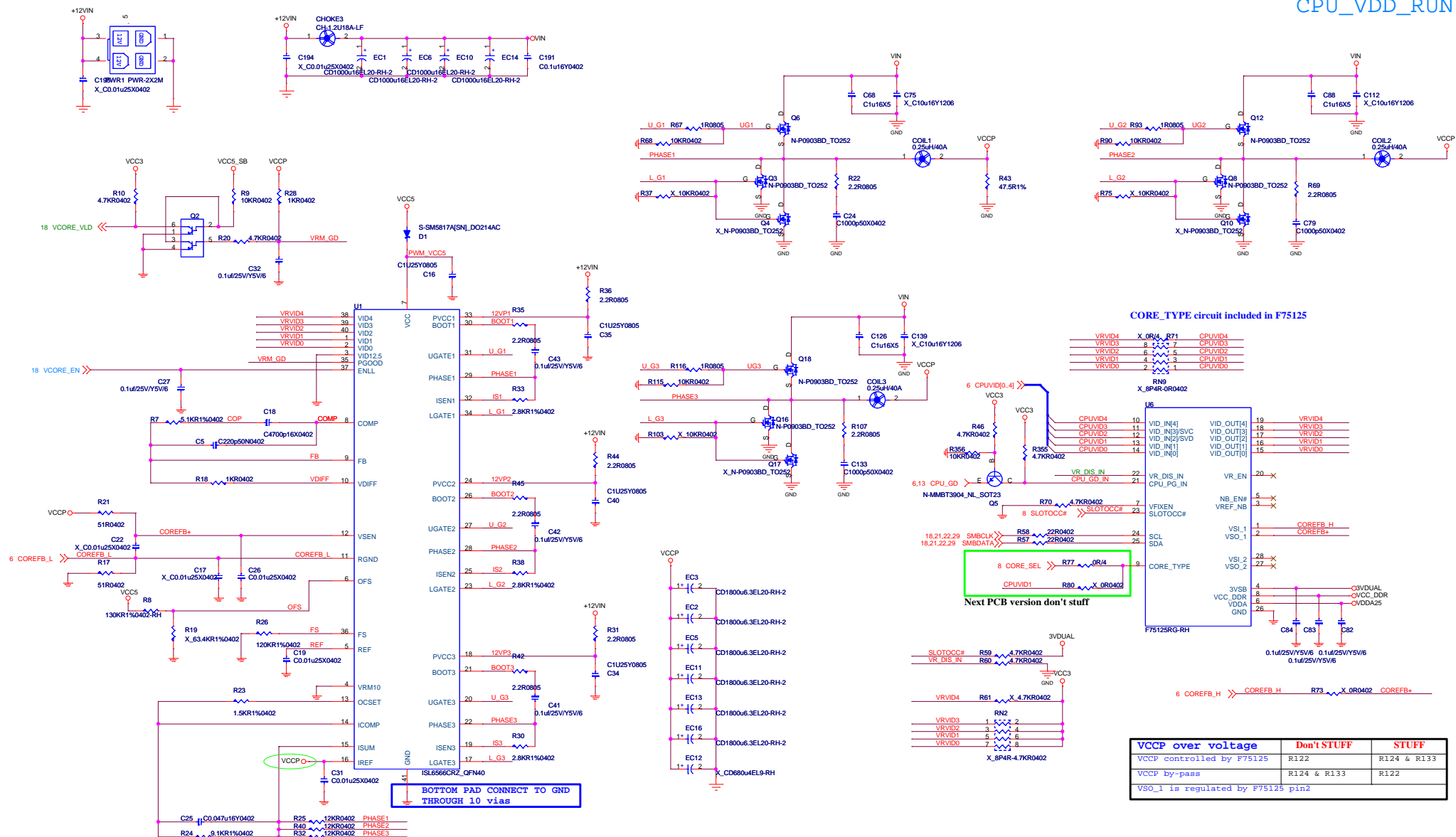
DDR II 1.8V POWER



DDR VTT Power

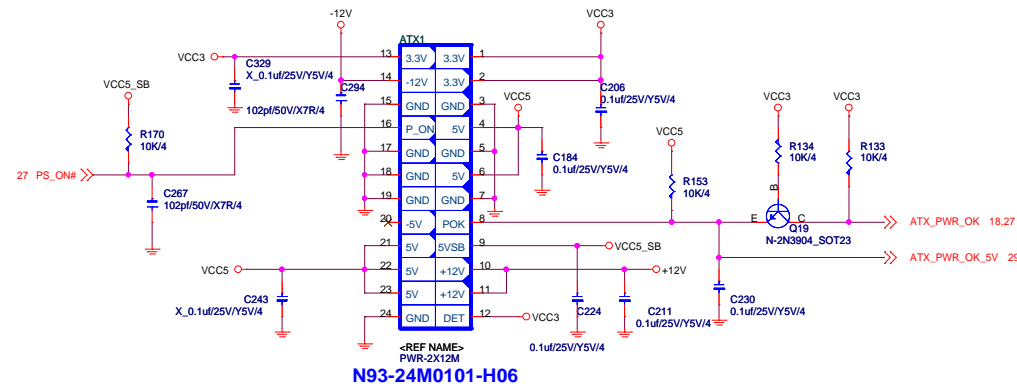


CPU_VDD_RUN

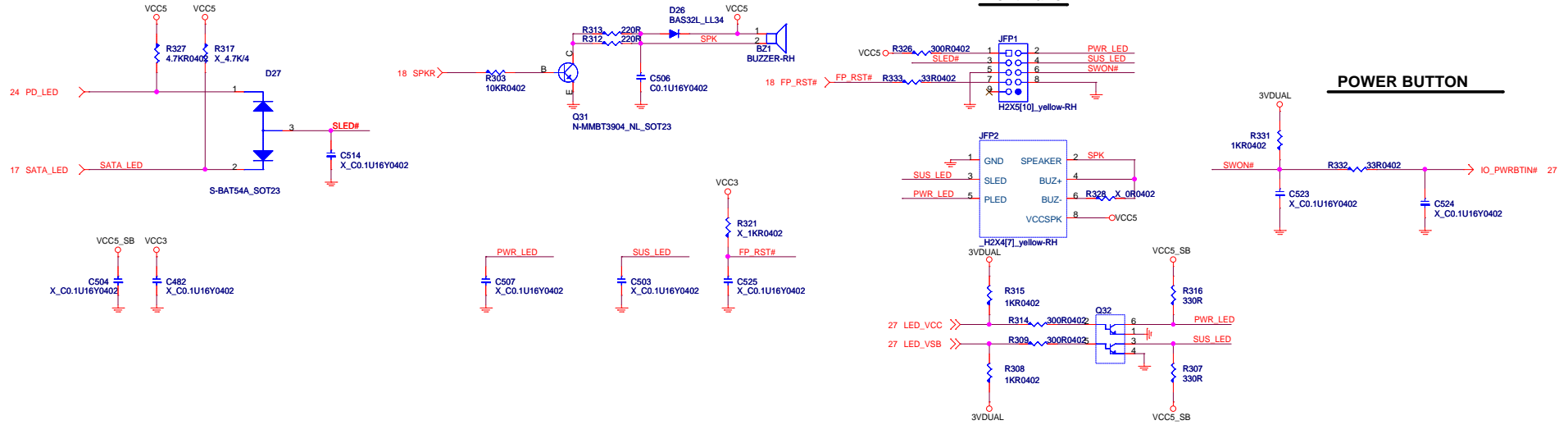


VCCP over voltage	Don't STUFF	STUFF
VCCP controlled by F75125	R122	R124 & R133
VCCP by-pass	R124 & R133	R122
VSO_1 is regulated by F75125 pin2		

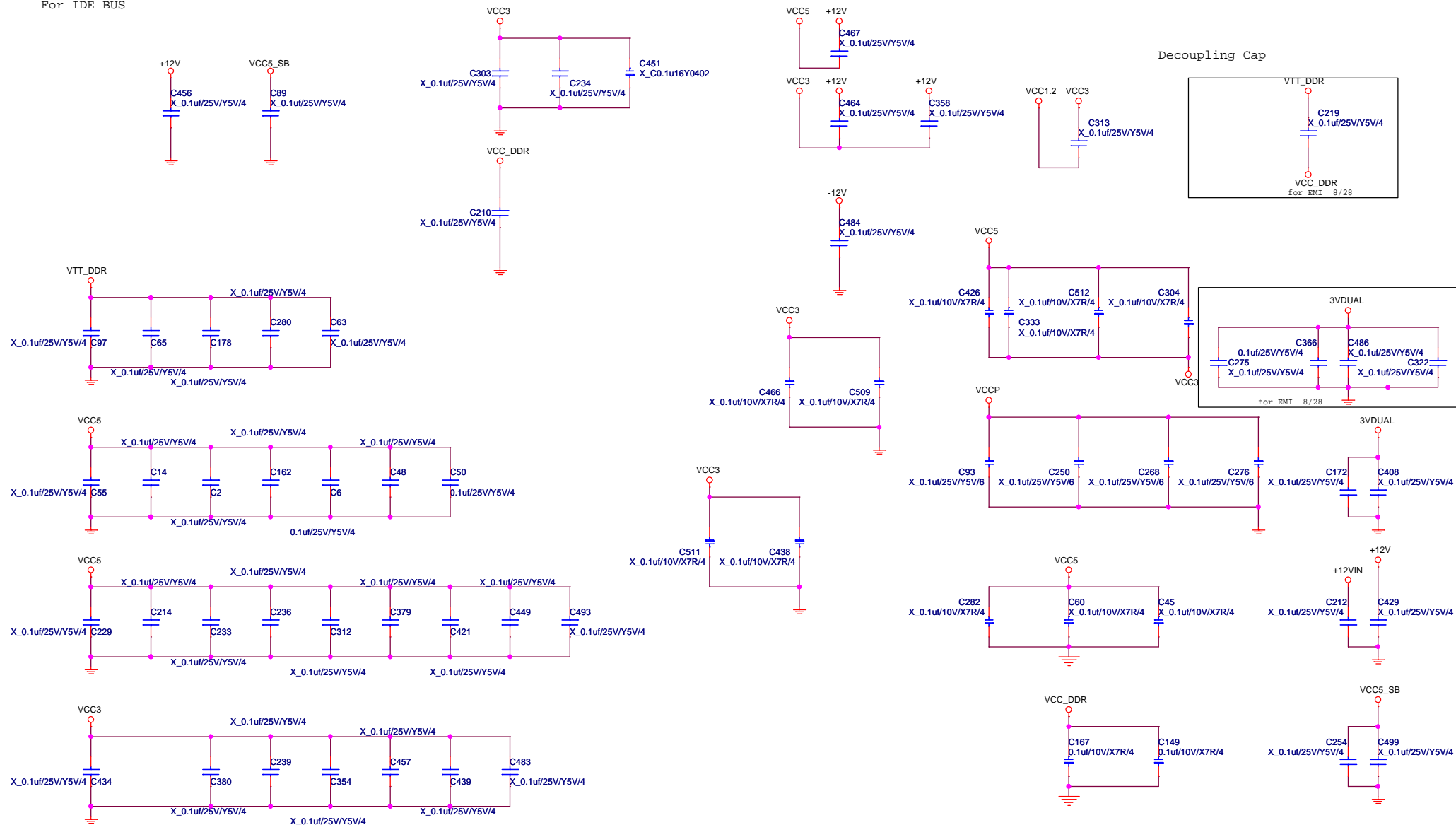
ATX Connector



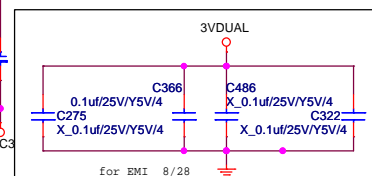
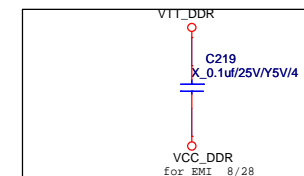
Front Panel




For IDE BUS

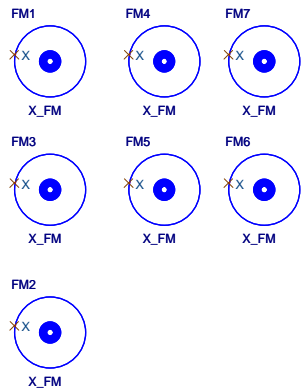


Decoupling Cap

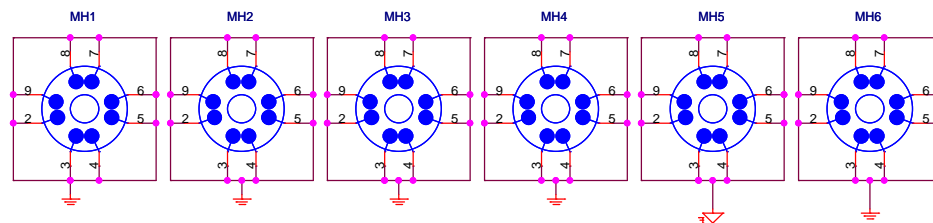


 MICRO-START INT'L CO.,LTD.			
Title			
FOR EMI			
Size B	Document Number	Rev	
	MS-7509	10	
Date:	Friday, January 11, 2008	Sheet	33 of 37

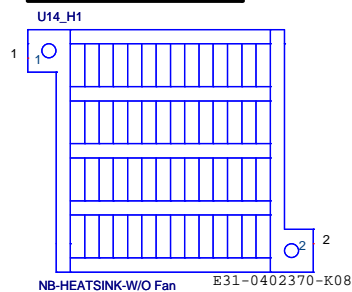
Optics Orientation Holes



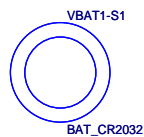
Mounting Holes



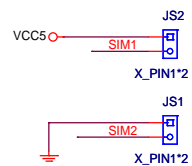
NB FAN/HEAT-SINK



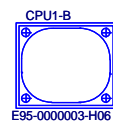
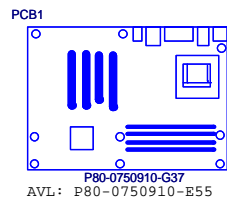
BATTERY




Simulation



PCB



		MICRO-START INTL CO.,LTD.	
Title		BOM - Option Parts	
Size	Document Number	Rev	
Custom	MS-7509	10	
Date:	Friday, January 11, 2008	Sheet	34 of 37

ATX P/S WITH 1A STBY CURRENT						CPU PW
VBAT	5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%	12V +/-5%

VRM SW
REGULATOR

CPU_VCORE (S0, S1)

VDD 1.5V
REGULATOR

VDD 1.3 V
REGULATOR

AM2 ATHLON 64	
VCORE	0.8-1.55V 80A(90W)
VTT_DDR	1.75A
VCC_DDR	3.6.A
VCC1_2HT	1.25V 0.5A

VTT_DDR(S0,S1,S3)
VCC_DDR(S0,S1,S3)
VCC1_2HT (S0, S1)

VCC1_2HT(S0,S1)

+3.3V (S0, S1)

MCP61

VCC1_2HT 1.3V 7.5A

VCC3 0.615A

3VDUAL 0.556A

1.2VDUAL 0.225A

VBAT(G3,S0,S1,S3,S4,S5)
VBAT 5mA(S0,S1)/
100uA(S3,S5)/
10uA(G3)

VTT_DDR(S0,S1,S3)

VCC_DDR(S0,S1,S3)

DDR400 DIMMs	
VTT_DDR	0.3A/DIMM (0.6A)
VCC_DDR	2.6A/DIMM (5.2A)

3VDUAL (S0, S1, S3, S4, S5)

1.2VDUAL (S0, S1, S3, S4, S5)

VBAT(G3,S0,S1,S3,S4,S5)

0.9V VTT_DDR
REGULATOR

1.8V VCC_DDR
REGULATOR

+3.3VDUAL REGULATOR
ACPI CONTROLLER

+5VSB REGULATOR
ACPI CONTROLLER

3VDUAL (S0, S1, S3, S4, S5)

+5V_Dual (S0, S1, S3)

1.2V STB
REGULATOR

1.2VDUAL (S0, S1, S3, S4, S5)

VBAT(G3,S0,S1,S3,S4,S5)

5VAA LDO
REGULATOR

+5VR (S0, S1)

VT6308P 1394	
VCC3	(S0, S1)

AC97 CODEC	
VCC3	(S0, S1)
+5VR	(S0, S1)

LAN	
3VDUAL	(S0, S1, S3, S4, S5)
AVDD18	
AVDD15	

SUPER I/O	
3VDUAL	(S0, S1, S3, S4, S5)
VCC3	(S0, S1)
VBAT	

3VDUAL (S0, S1, S3, S4, S5)

VCC3 (S0, S1)

VBAT

+5V_Dual (S0, S1, S3)

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X2

X1 PCIE		X16 PCIE	
3.3V	3.0A	3.3V	3.0A
12V	5.5A	12V	5.5A

1394 FR*1		1394 RL*1	
12V	1.5A	12V	1.5A

USB FR*4	
5VDual	2A

USB RL*4	
5VDual	2A

PS/2	
5VDual	1A

+3.3VDUAL (S0, S1, S3)

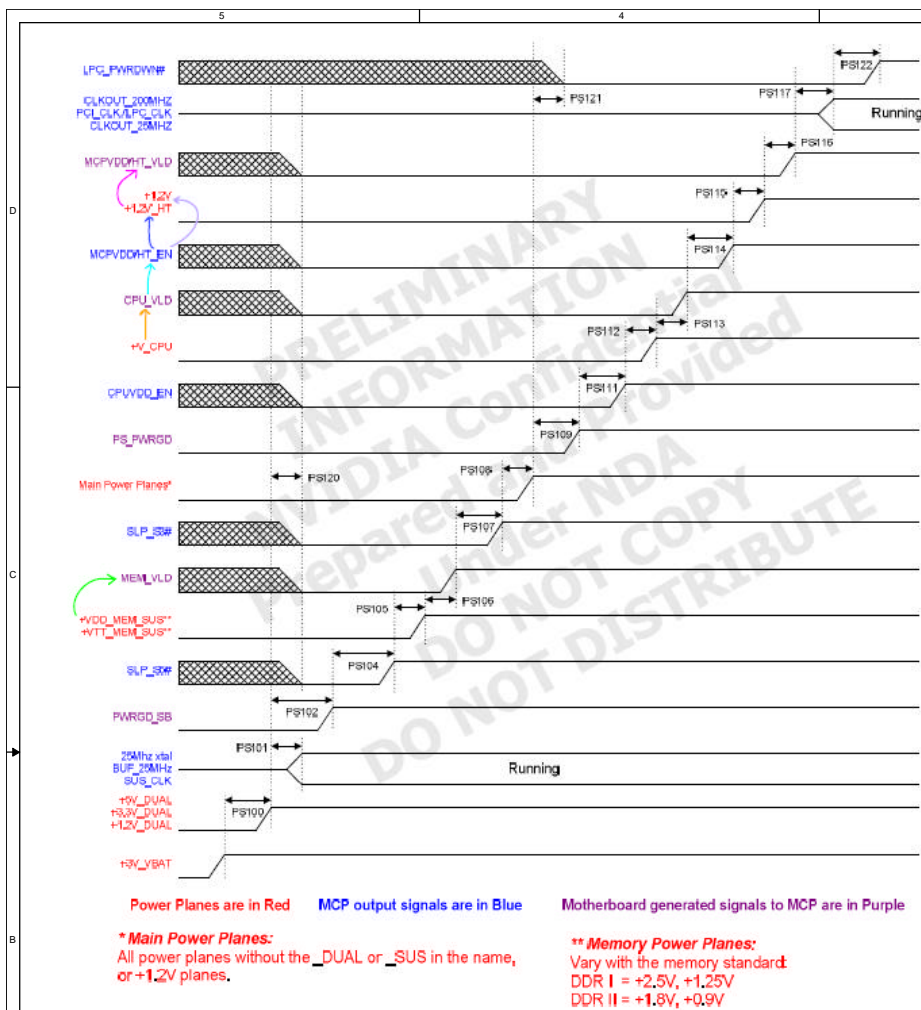


Figure 4-2. MCP68 G3-to-S0 Power-Up Sequence

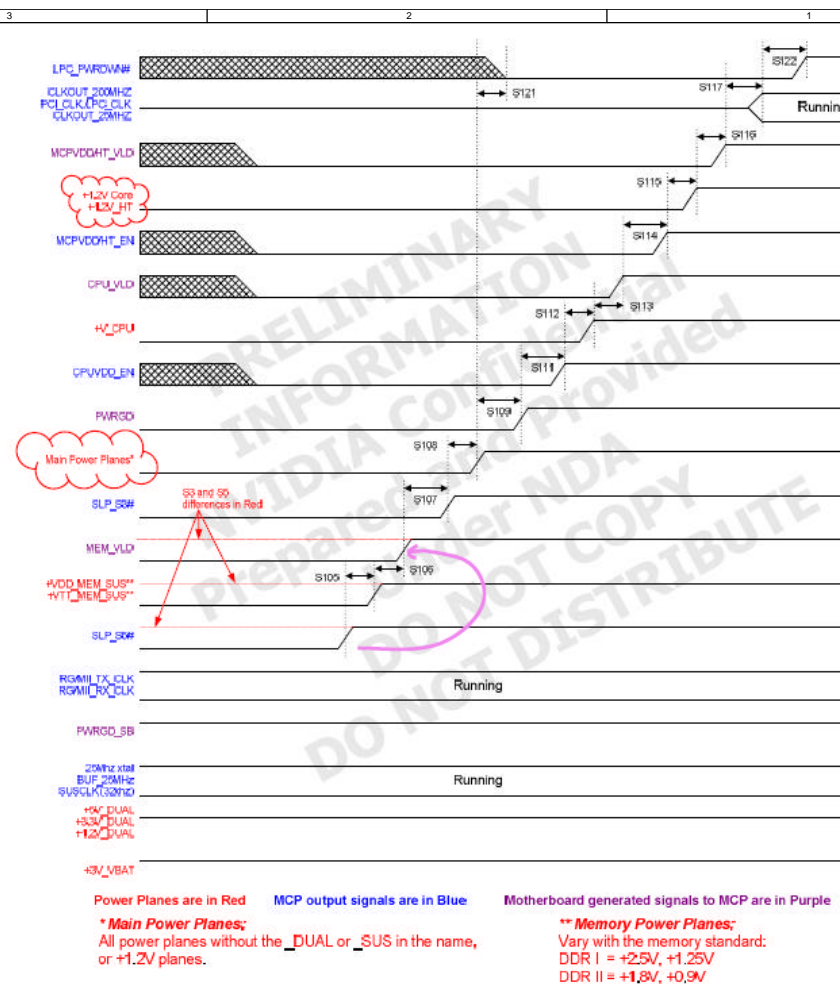



Figure 4-3. MCP68 S3/S4/S5 Power Resume Sequence

2008/1/10 0A CHANGE 10

項 目	原 因	元 件
1	AMD CPU request	Add R354 and R191
2	for NVIDAI circuit D version	U14 V22 pin circuit modify
3	for no JMP381 install	Add R196
4	for UPI7501 挑 700W power	Q33 and Q34 and R350 and R351 and R352
5	for chipset ver:A2 circuit modify	Q27, Q28 , R228, R233, R329, R234 , R349 and add R16,R320
6	signal quality	R244 and R245
7	HT_VLD and VCC1.2 timing	R319 and C422
8	G3 to G5 VCC_DDR have power output	Add Q36, D32, R322, R323

 MICRO-START INT'L CO.,LTD.		
Title HISTORY		
Size Custom	Document Number MS-7509	Rev 10
Date: Friday, January 11, 2008 Sheet 37 of 37		